

X470 AORUS ULTRA GAMING

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2015.12.30~B.L

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Title

COVER SHEET

Size Custom

Document Number


X470 AORUS ULTRA GAMING

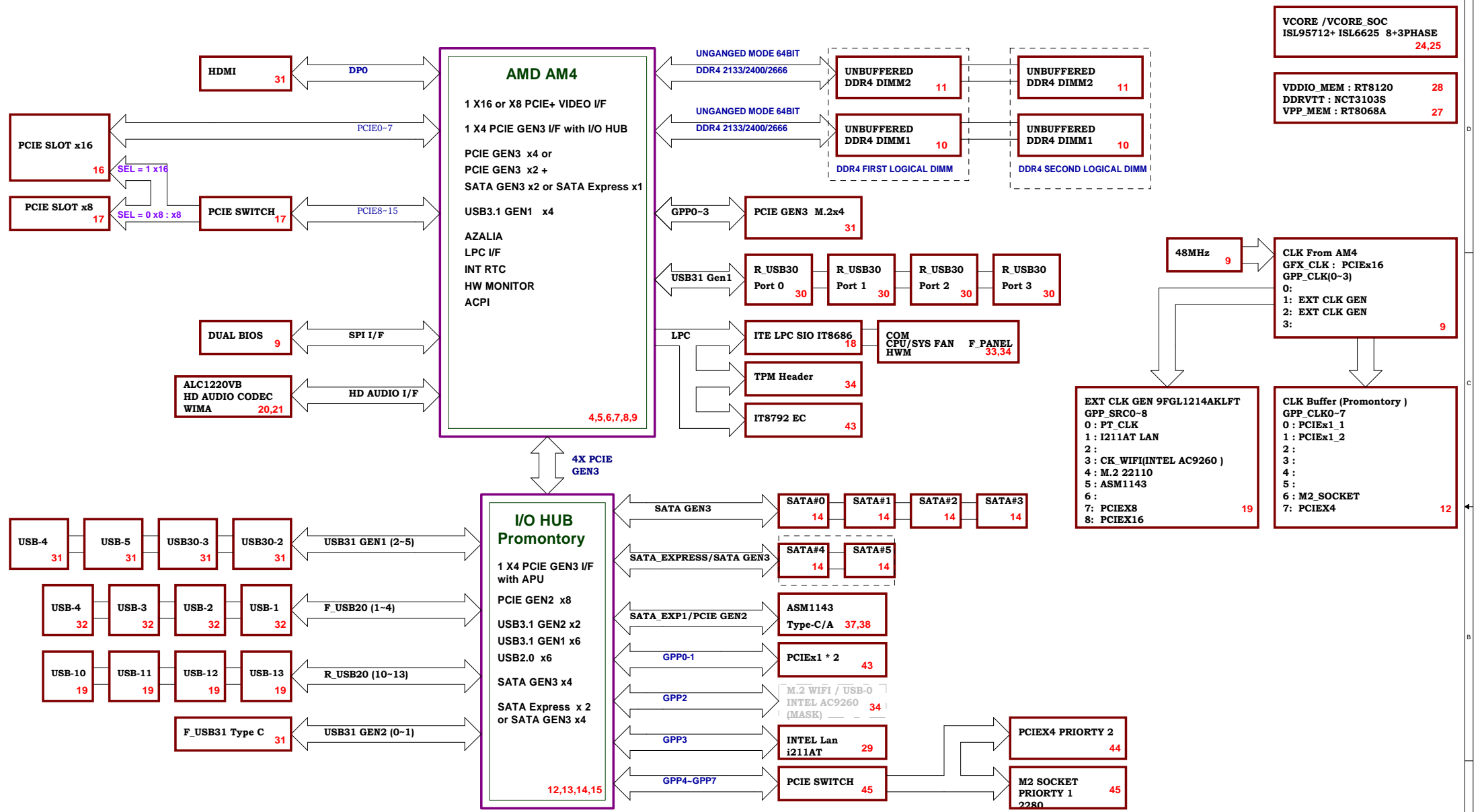
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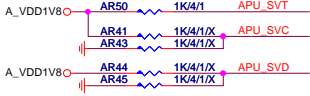
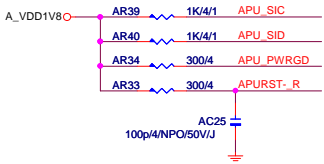
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Date: Tuesday, February 13, 2018

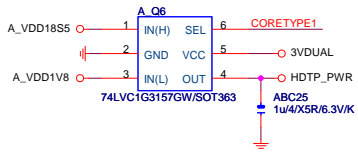
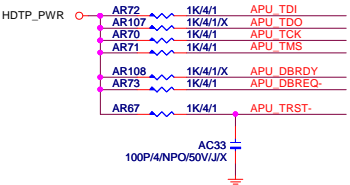
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Title			
<p align="center">BOM & PCB HISTORY</p>			
Size	Document Number	Rev	
Custom	X470 AORUS ULTRA GAMING	1.0	
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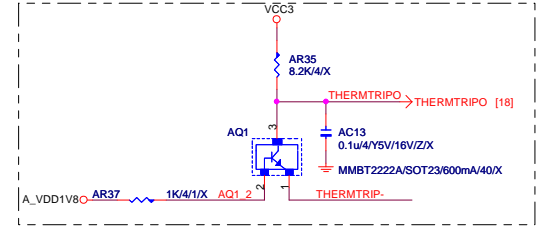
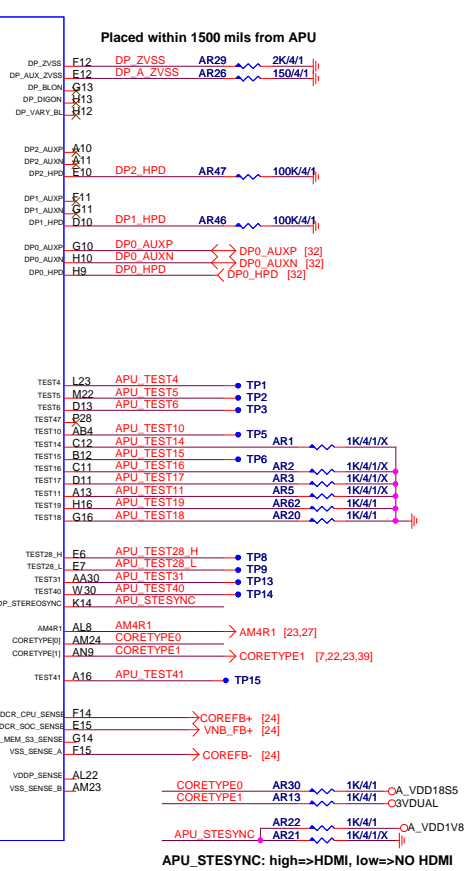
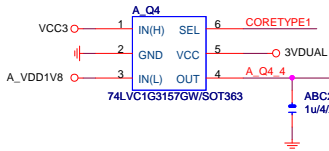
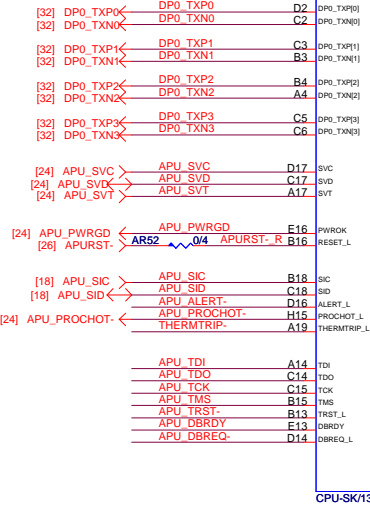




SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



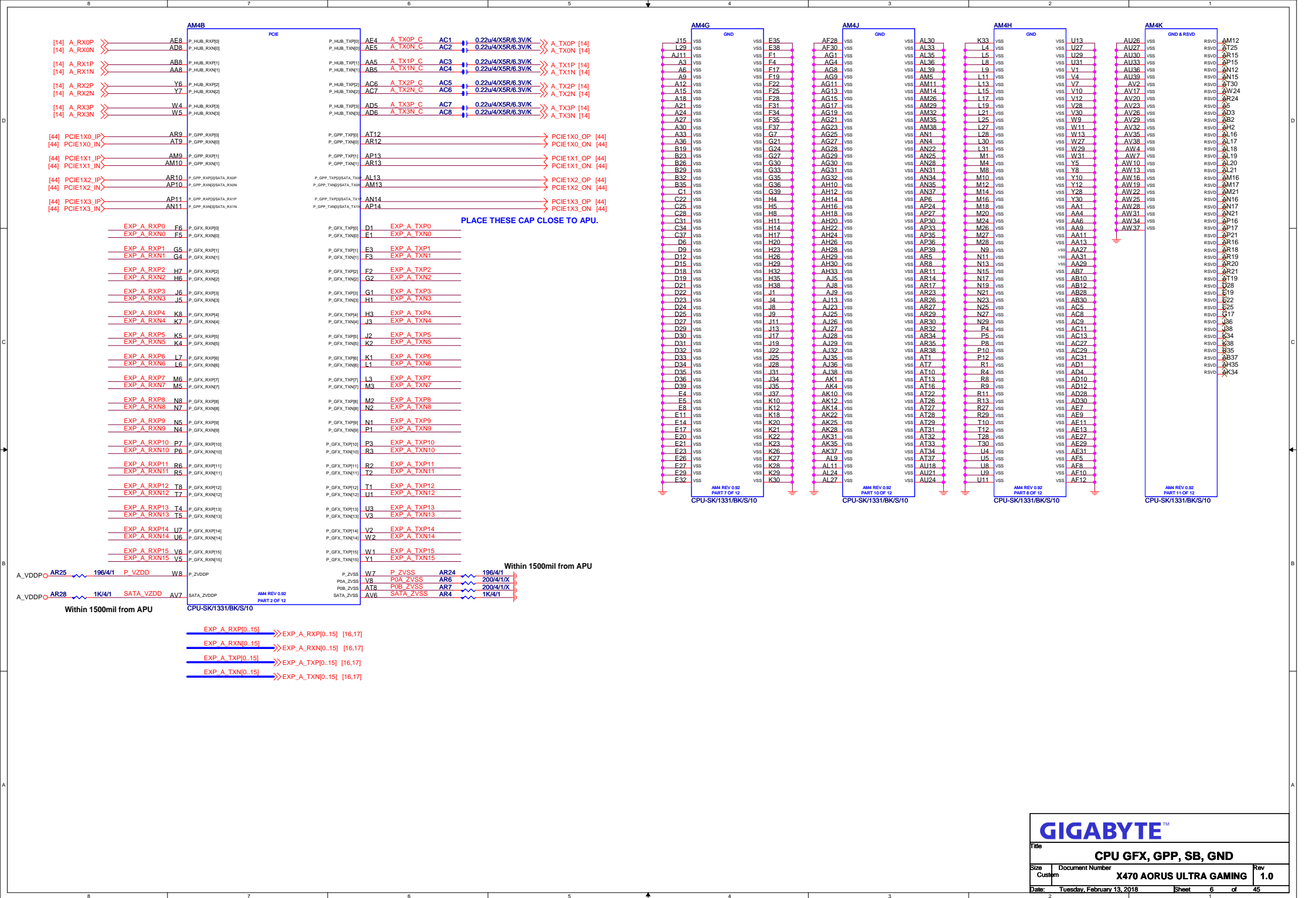
HDMI



APU_STESYNC: high=>HDMI, low=>NO HDMI

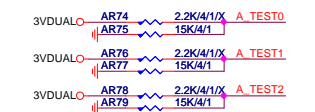
CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0	1	Reserved	TYPE 1
1 ST	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

GIGABYTE™			
Title CPU DDI, CONTROL			
Size Custom	Document Number X470 AORUS ULTRA GAMING	Rev 1.0	
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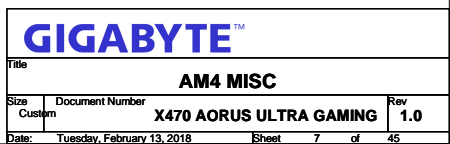
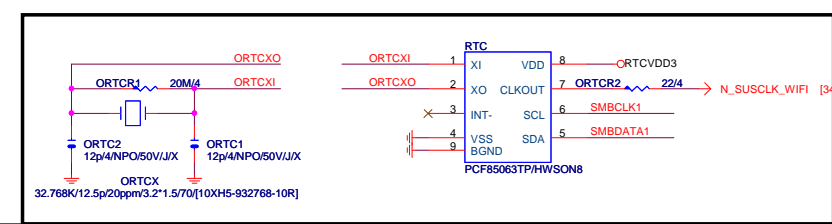
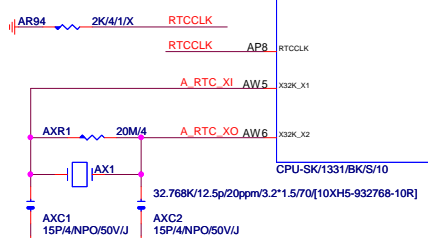
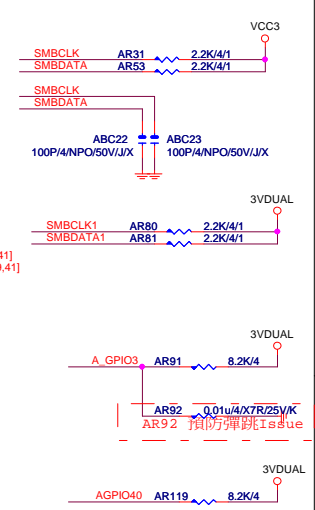
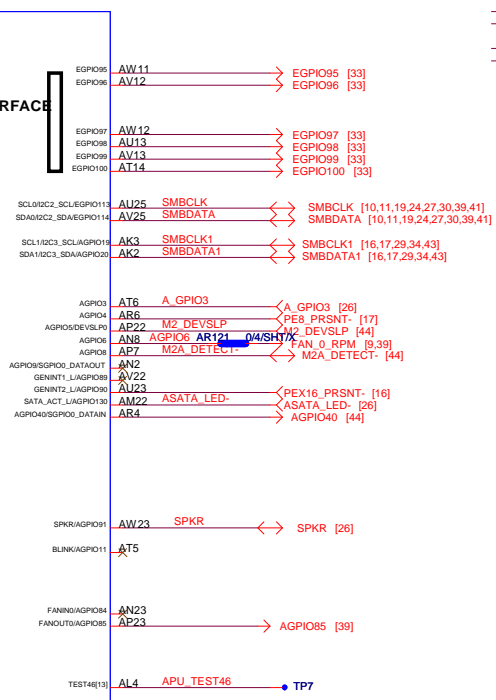
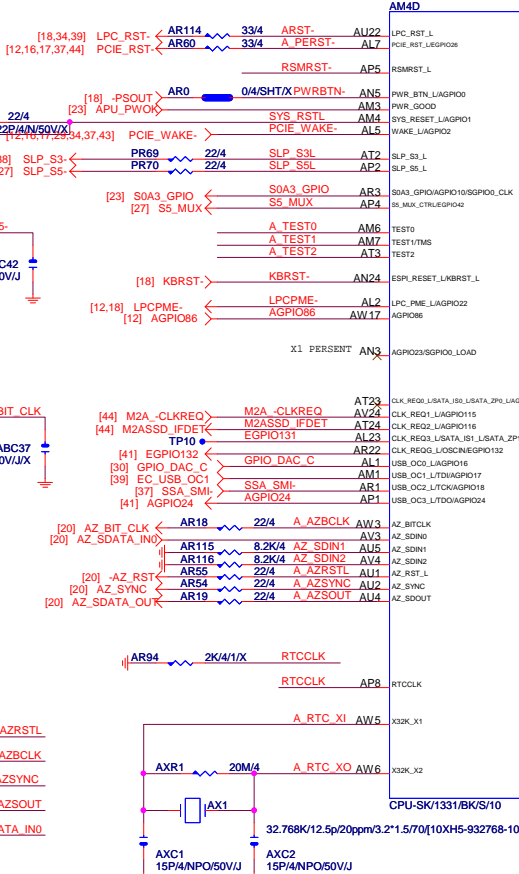
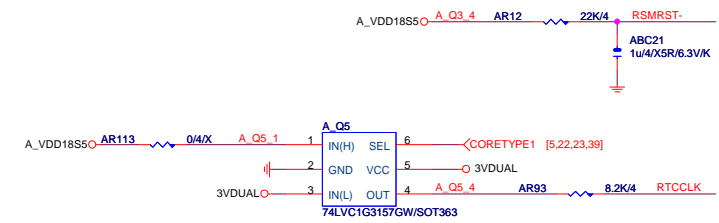
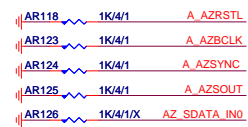


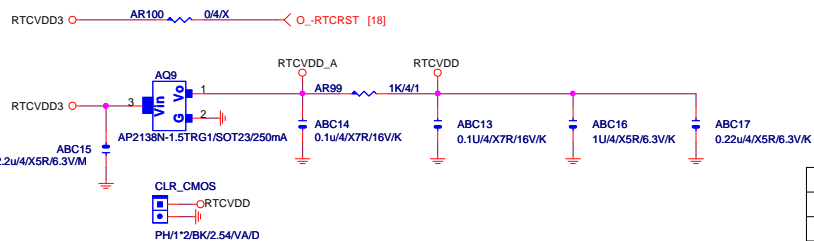
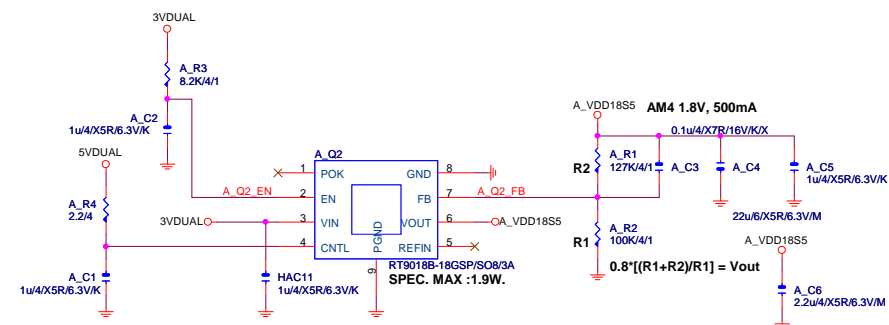
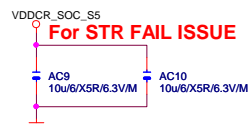
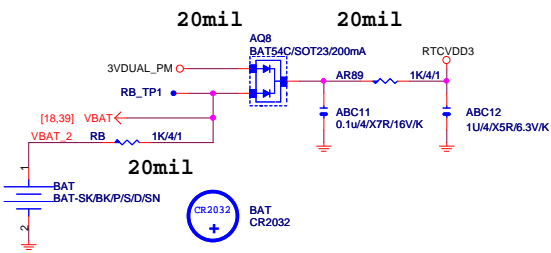
Pinmux diagram for the i.MX6Q processor. The diagram shows 16 pins (3VDUAL0 to 3VDUAL15) connected to various functions. The connections are as follows:

- 3VDUAL0: AR95, 8.2K/4/X, SYS_RSTL
- 3VDUAL1: AR96, 1K/1/1/X, SYS_RSTL
- 3VDUAL2: AR103, 8.2K/4/X, PCIE_RST-
- 3VDUAL3: AR120, 8.2K/4/X, PCIE_RST-
- VCC330: AR104, 8.2K/4/X, PCIE_WAKE-
- 3VDUAL4: AR104, 8.2K/4/X, PCIE_WAKE-
- 3VDUAL5: AR112, 1K/4/1/X, S0A3_GPIO
- 3VDUAL6: AR111, 8.2K/4/X, LPMC_P3-
- 3VDUAL7: AR110, 1K/4/1/X, SLP_S3-
- 3VDUAL8: AR110, 1K/4/1/X, SLP_S3-
- 3VDUAL9: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL10: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL11: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL12: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL13: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL14: AR109, 1K/4/1/X, SLP_S5-
- 3VDUAL15: AR109, 1K/4/1/X, SLP_S5-



TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



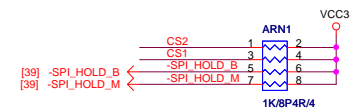
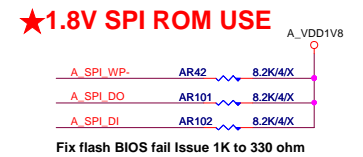
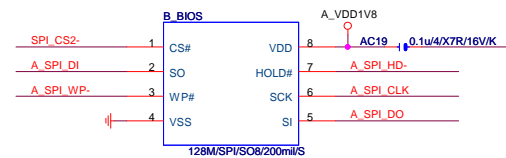
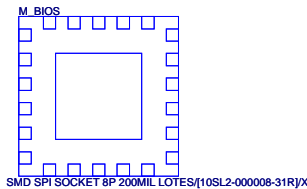
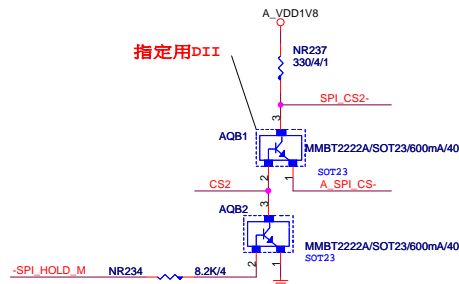
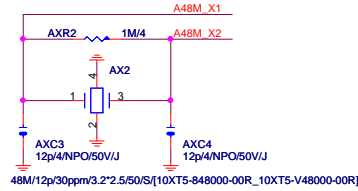


AMD SK1331/BK/S/10

Vcore EDC =1.25V
Vcore 0.75-1.2V

Vcore SOC EDC=75A
Vcore SOC 0.75-1.2V

CPU-SK1331/BK/S/10

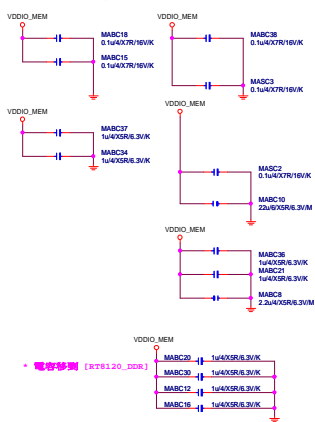




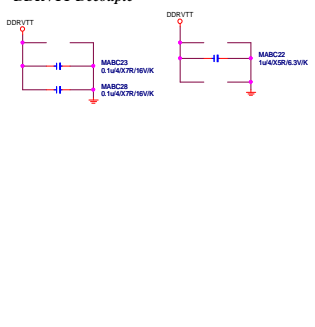
CHANNEL A0
SA2:0=000
黑色DIMM NO Shield
Footprints: 保留STH 加強版

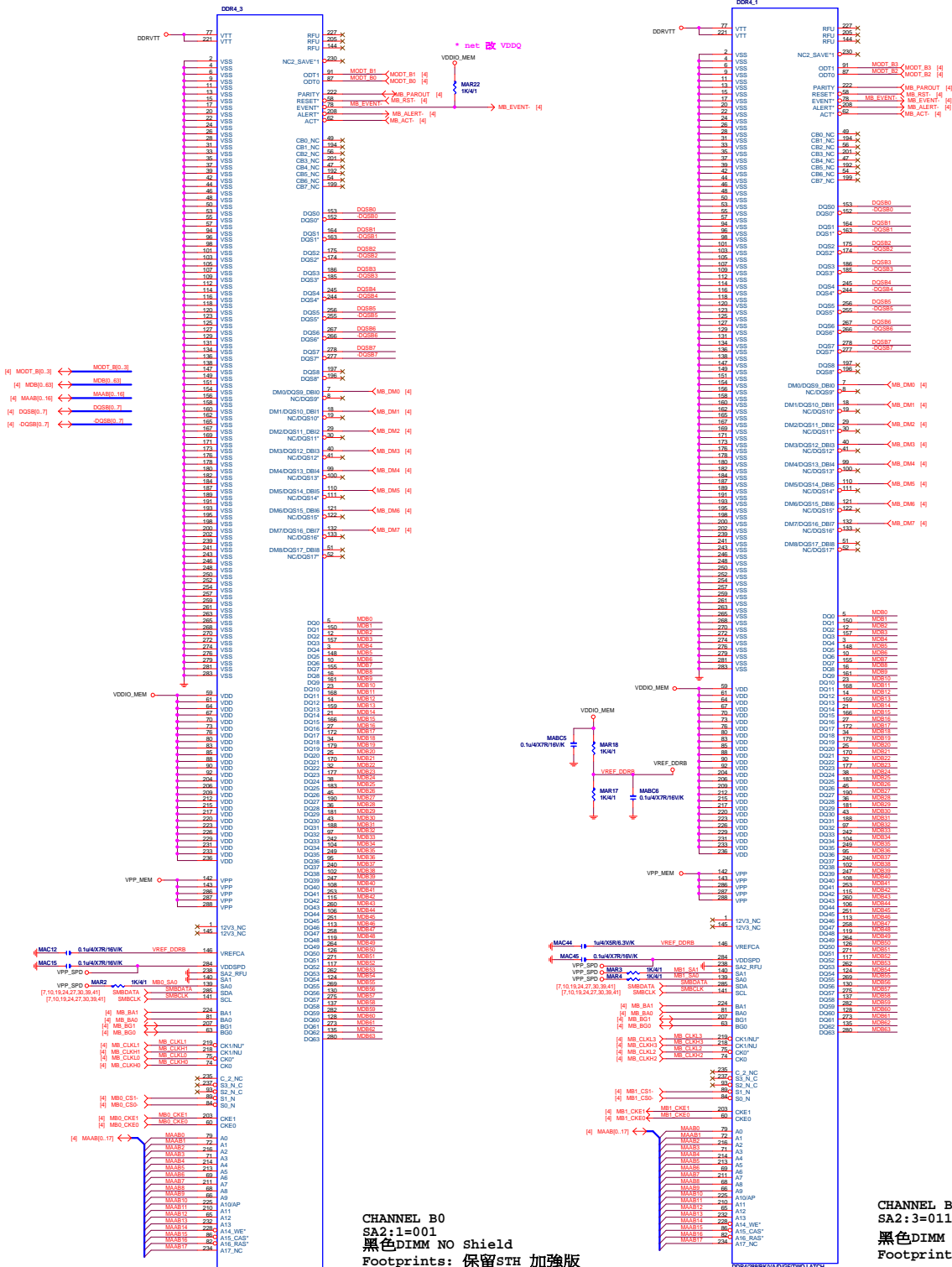


CHANNEL A1
SA2:2=010
黑色DIMM NO Shield
Footprints: 保留STH 加強版

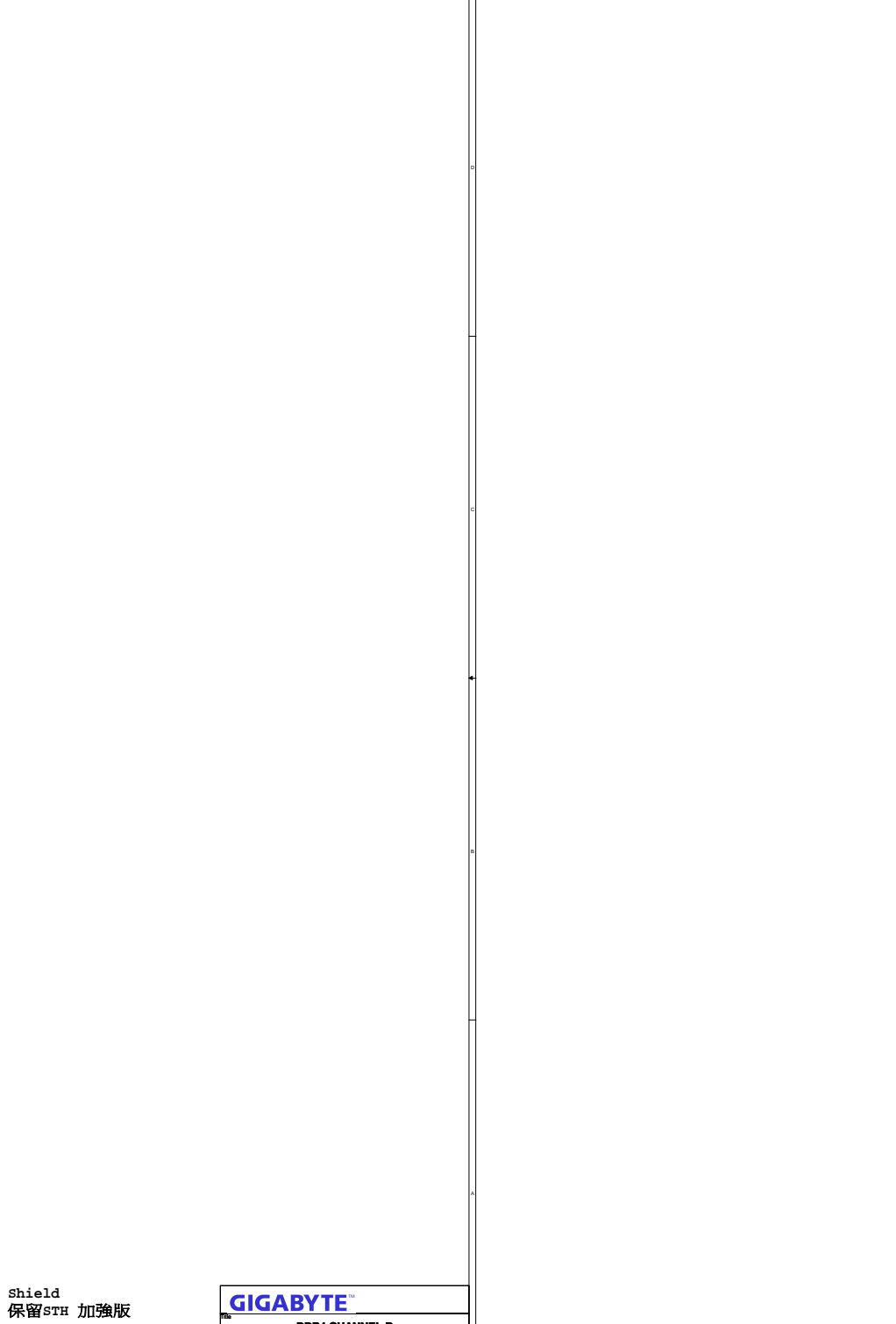


DDRVTT Decouple

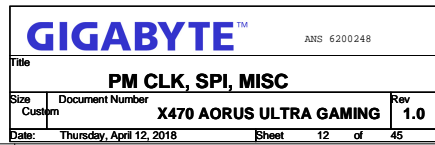


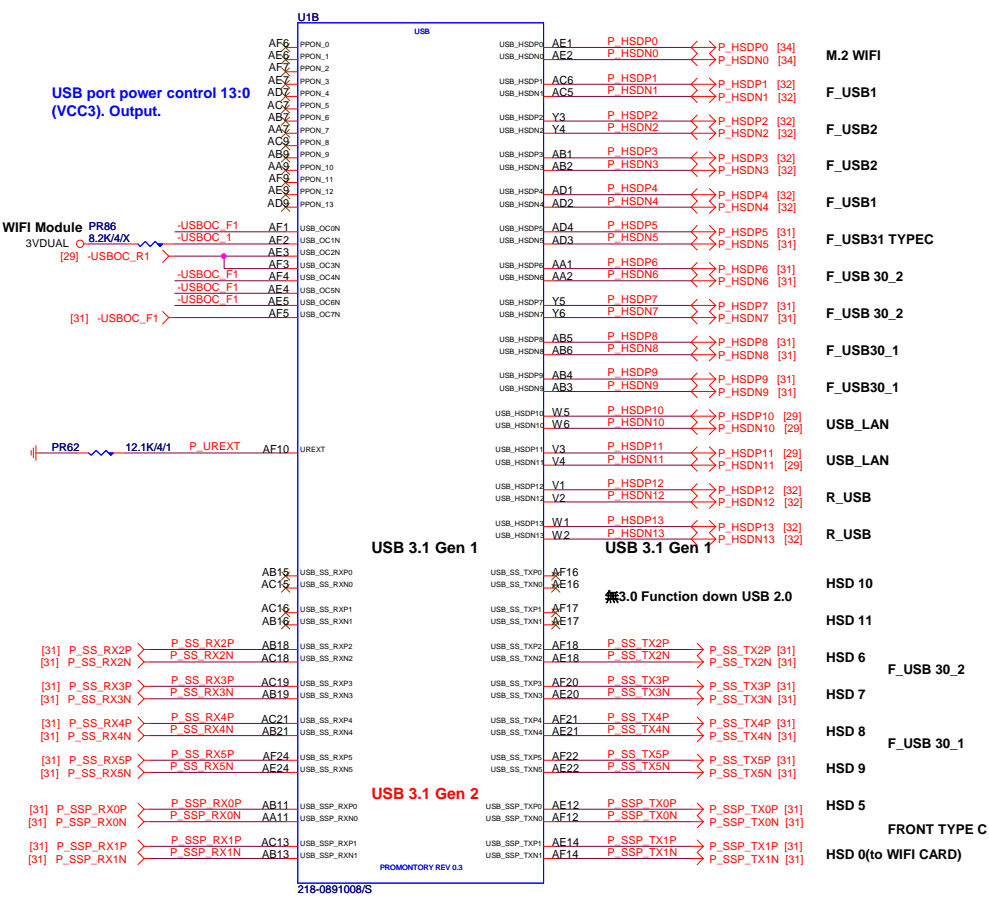


CHANNEL B0
SA2:1=001
黑色DIMM NO Shield
Footprints: 保留STH 加強版



CHANNEL B1
SA2:3=011
黑色DIMM NO shield
Footprints: 保留STH 加強版

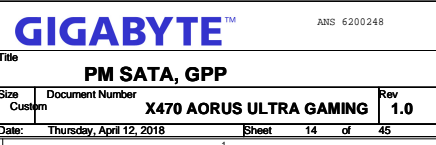


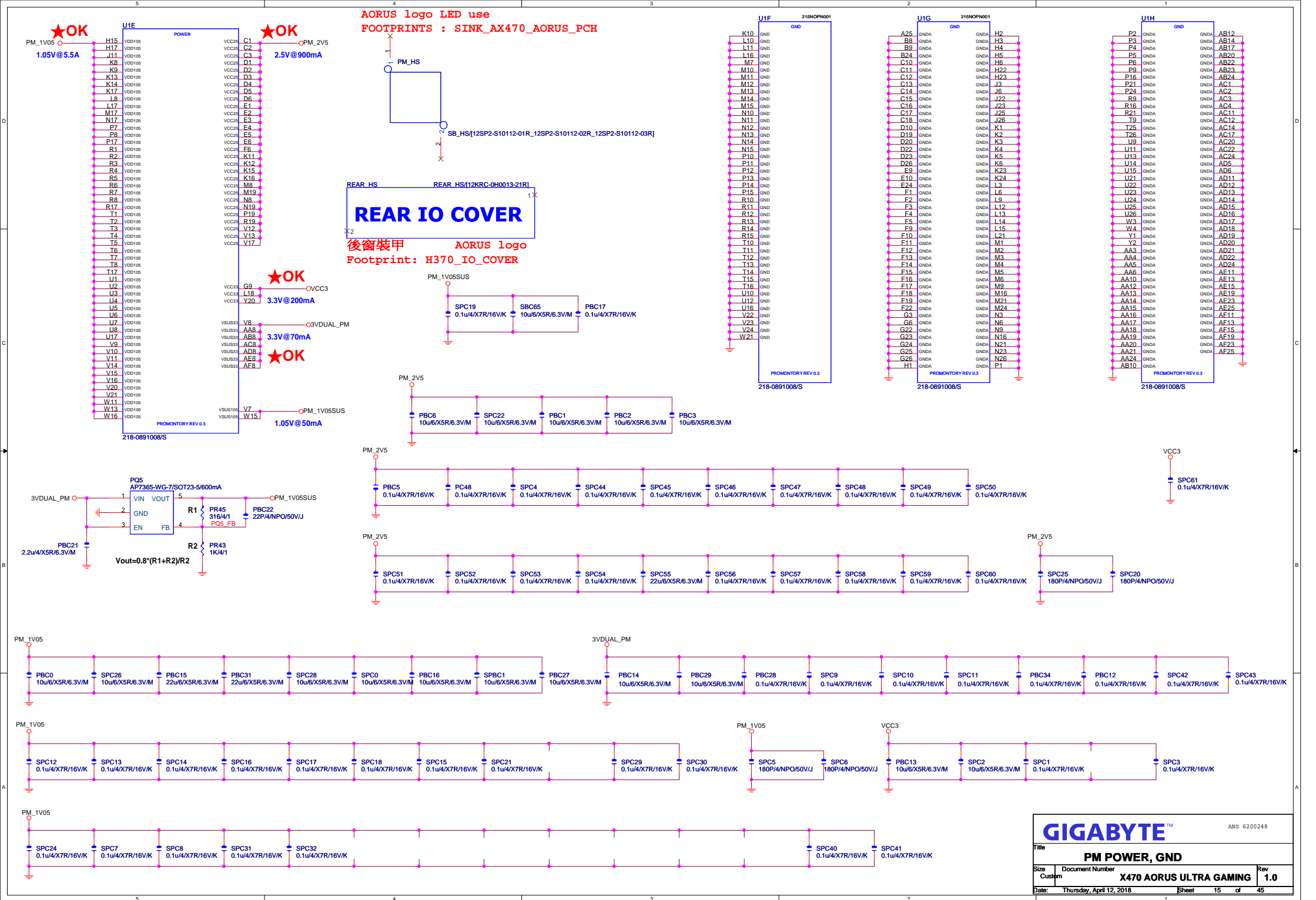


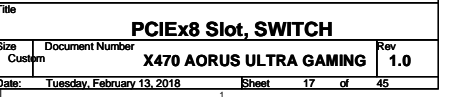
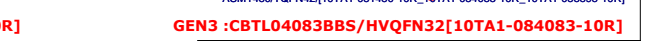
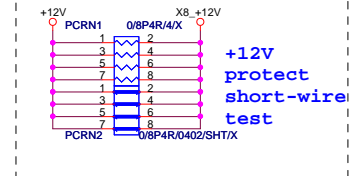
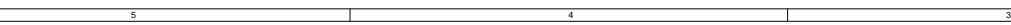
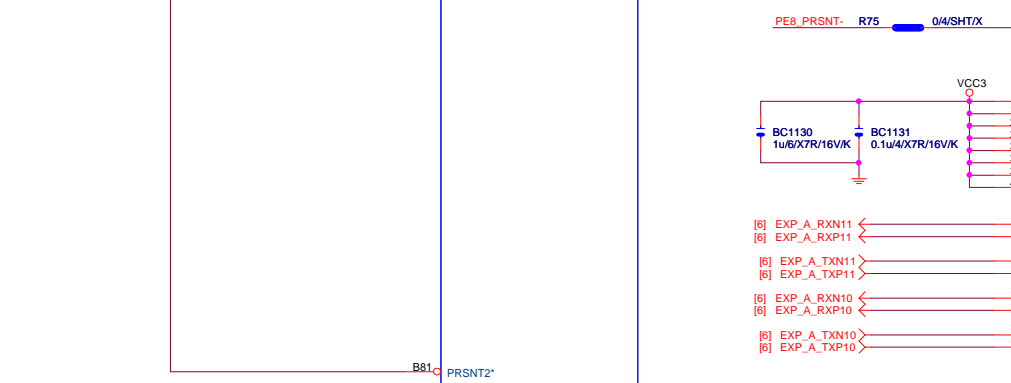
AE1	P_HSDP0	→	P_HSDP0	[34]	M.2 WIFI
AE2	P_HSDN0	↔	P_HSDN0	[34]	
AC6	P_HSDP1	→	P_HSDP1	[32]	F_USB1
AC5	P_HSDN1	↔	P_HSDN1	[32]	
Y3	P_HSDP2	→	P_HSDP2	[32]	F_USB2
Y4	P_HSDN2	↔	P_HSDN2	[32]	
AB1	P_HSDP3	→	P_HSDP3	[32]	F_USB2
AB2	P_HSDN3	↔	P_HSDN3	[32]	
AD1	P_HSDP4	→	P_HSDP4	[32]	F_USB1
AD2	P_HSDN4	↔	P_HSDN4	[32]	
AD4	P_HSDP5	→	P_HSDP5	[31]	F_USB31 TYPEC
AD3	P_HSDN5	↔	P_HSDN5	[31]	
AA1	P_HSDP6	→	P_HSDP6	[31]	F_USB 30_2
AA2	P_HSDN6	↔	P_HSDN6	[31]	
Y5	P_HSDP7	→	P_HSDP7	[31]	F_USB 30_2
Y6	P_HSDN7	↔	P_HSDN7	[31]	
AB5	P_HSDP8	→	P_HSDP8	[31]	F_USB30_1
AB6	P_HSDN8	↔	P_HSDN8	[31]	
AB4	P_HSDP9	→	P_HSDP9	[31]	F_USB30_1
AB3	P_HSDN9	↔	P_HSDN9	[31]	
W5	P_HSDP10	→	P_HSDP10	[29]	USB_LAN
W6	P_HSDN10	↔	P_HSDN10	[29]	
V3	P_HSDP11	→	P_HSDP11	[29]	USB_LAN
V4	P_HSDN11	↔	P_HSDN11	[29]	
V1	P_HSDP12	→	P_HSDP12	[32]	R_USB
V2	P_HSDN12	↔	P_HSDN12	[32]	
W1	P_HSDP13	→	P_HSDP13	[32]	R_USB
W2	P_HSDN13	↔	P_HSDN13	[32]	
AF16	P_SS_TX0P	→	P_SS_TX0P	[31]	HSD 10
AE16	P_SS_TX0N	→	P_SS_TX0N	[31]	
AF17	P_SS_TX1P	→	P_SS_TX1P	[31]	HSD 11
AE17	P_SS_TX1N	→	P_SS_TX1N	[31]	
AF18	P_SS_TX2P	→	P_SS_TX2P	[31]	HSD 6
AE18	P_SS_TX2N	→	P_SS_TX2N	[31]	
AF20	P_SS_TX3P	→	P_SS_TX3P	[31]	F_USB 30_2
AE20	P_SS_TX3N	→	P_SS_TX3N	[31]	
AF21	P_SS_TX4P	→	P_SS_TX4P	[31]	HSD 7
AE21	P_SS_TX4N	→	P_SS_TX4N	[31]	
AF22	P_SS_TX5P	→	P_SS_TX5P	[31]	HSD 8
AE22	P_SS_TX5N	→	P_SS_TX5N	[31]	
AE12	P_SSP_TX0P	→	P_SSP_TX0P	[31]	HSD 9
AE12	P_SSP_TX0N	→	P_SSP_TX0N	[31]	
AE14	P_SSP_TX1P	→	P_SSP_TX1P	[31]	HSD 5
AE14	P_SSP_TX1N	→	P_SSP_TX1N	[31]	

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0







for LPC/eSPI power mode

SIO STRAP

SIO STRAP


OR33 1K/4/1 JP2 8.2K/4 VCC3

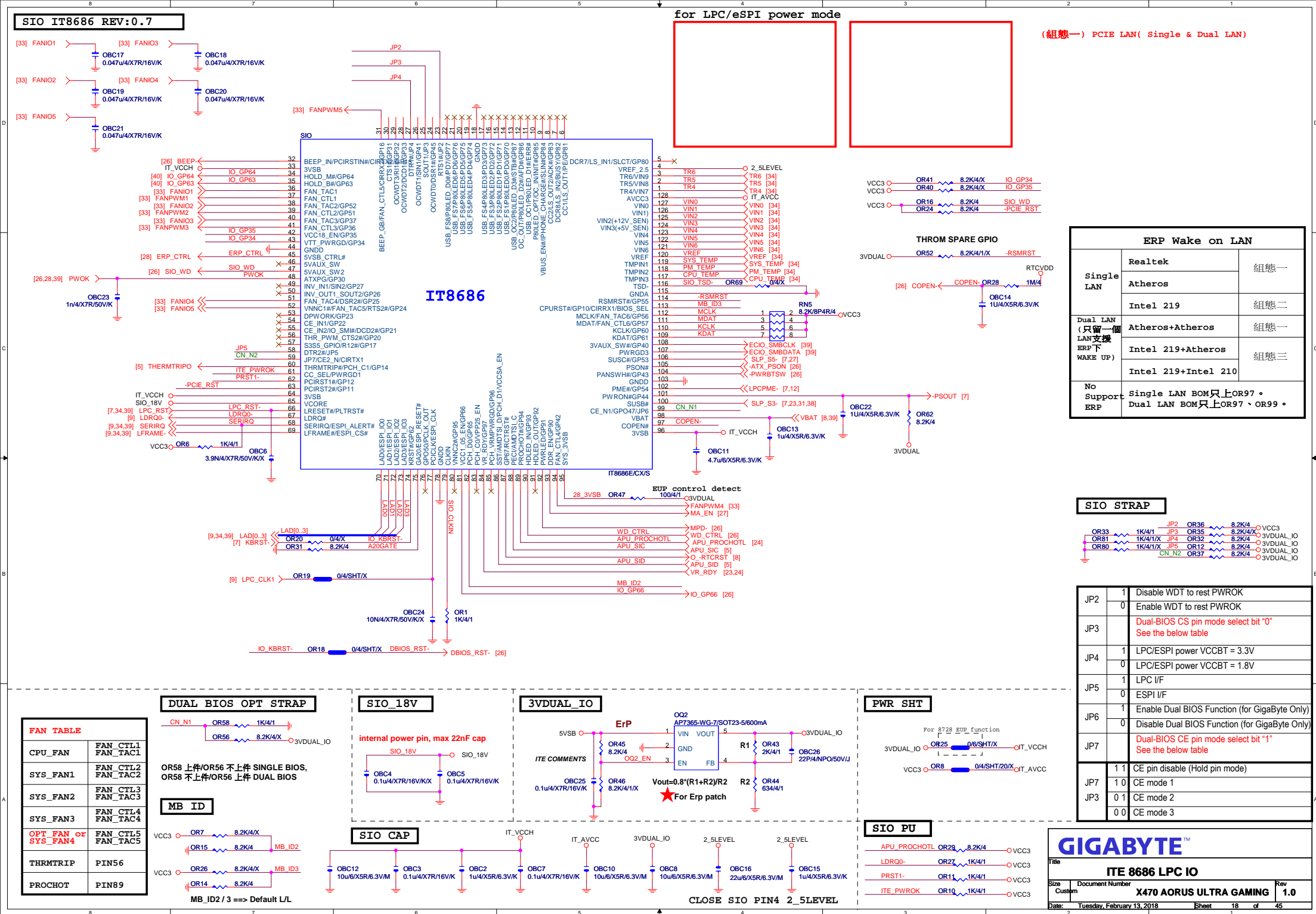
OR81 1K/4/1/X JP3 8.2K/4/X 3VDUAL_IO

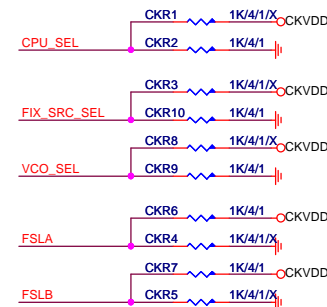
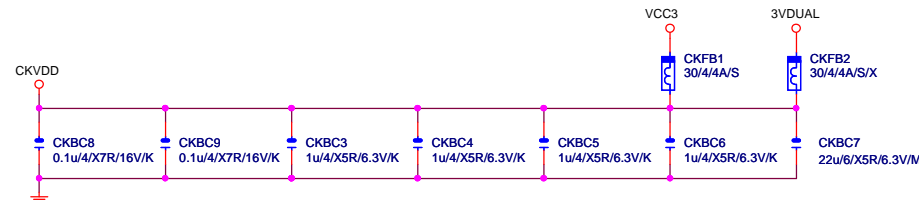
OR80 1K/4/1/X JP4 8.2K/4 3VDUAL_IO

JP5 8.2K/4 3VDUAL_IO

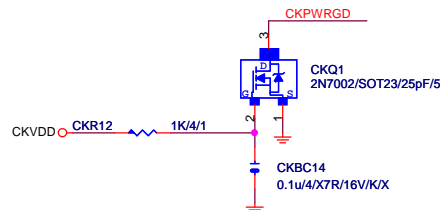
CN_N2 OR37 8.2K/4 3VDUAL_IO


			
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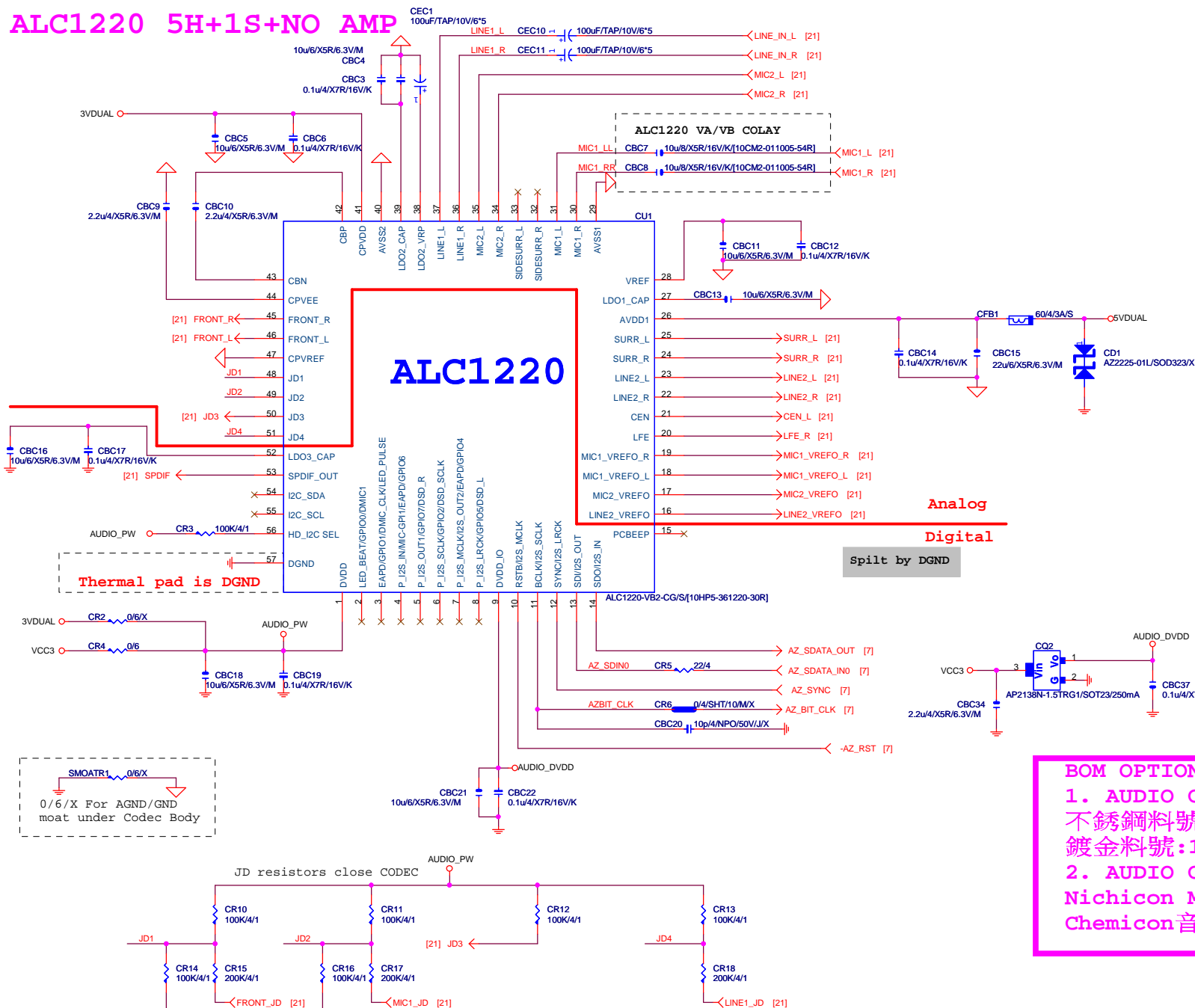


FSLB	FSLA	BCLK
1	1	100M
1	0	125M
0	1	166M
0	0	250M



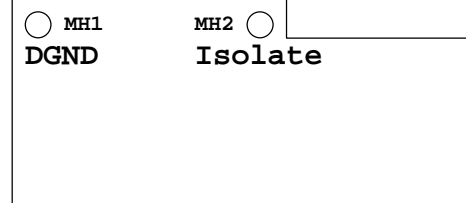
			
Title			
IDT CKG			
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ALC1220 5H+1S+NO AMP



LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate

LAYOUT注意:是否要加?
AGND切割線

BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

鍍金料號:11NR6-403025-92R

2. AUDIO CAP

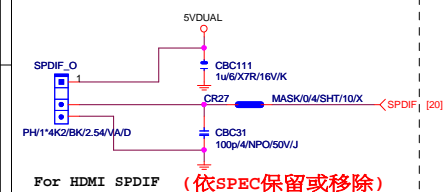
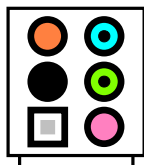
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Chemicon音效電容 : 11CE2-651000-05R

GIGABYTE™

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AZALIA JACK



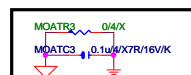
For HDMI SPDIF (依SPEC保留或移除)



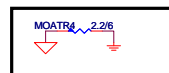
► Near F_AUDIO



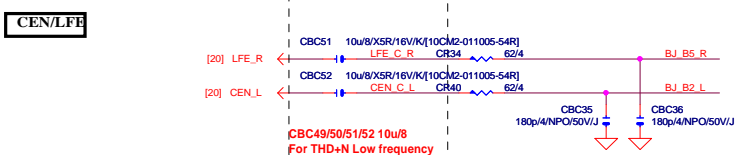
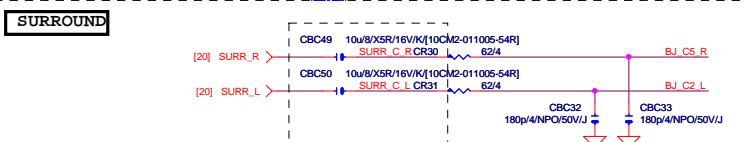
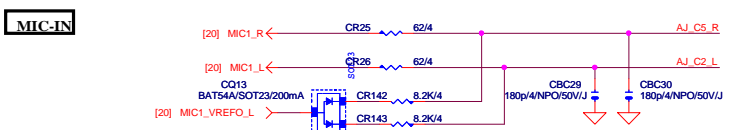
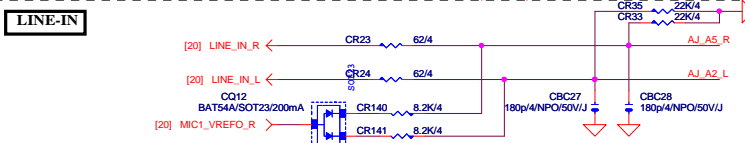
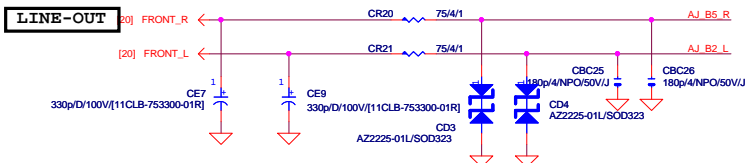
► Near Codec



► Under Audio Jack

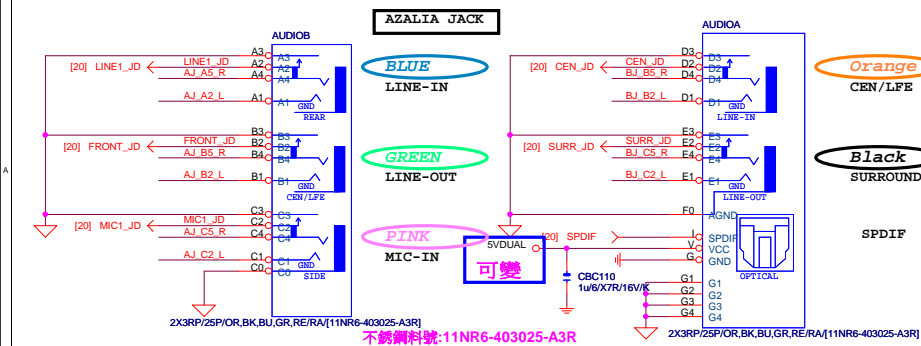
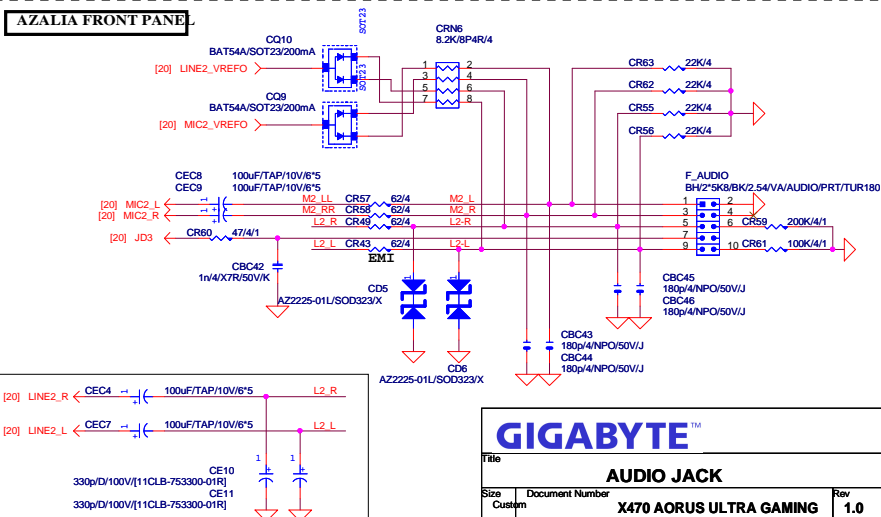
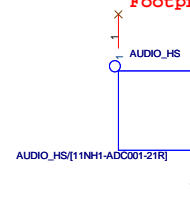


► Audio Jack - LAN



AUDIO 鐵殼

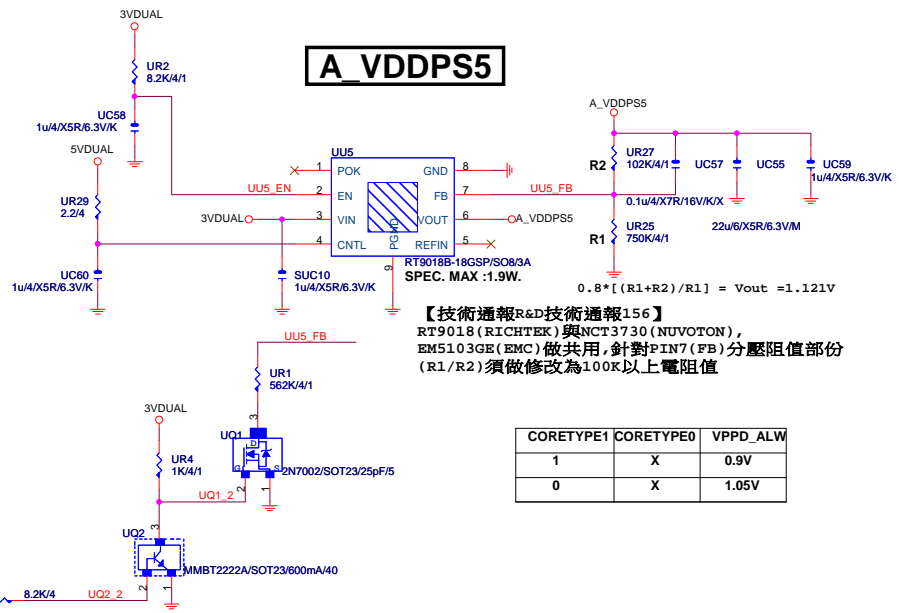
Footprint: AUDIO_COVER-1



不銹鋼料號:11NR6-403025-A3R
鍍金料號:11NR6-403025-92R

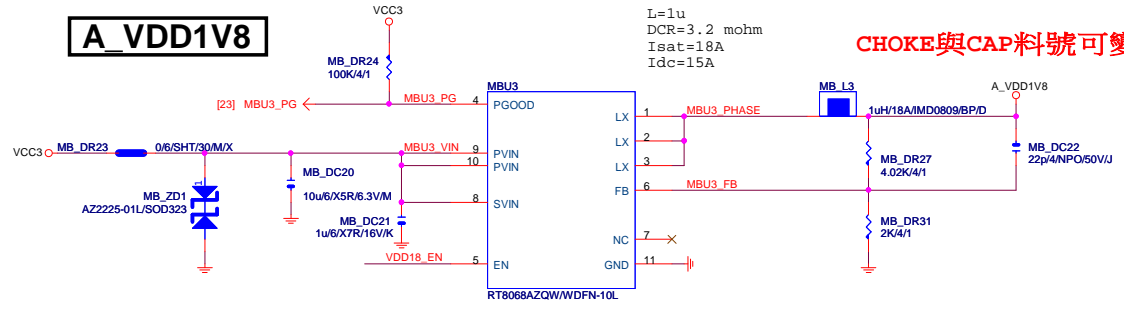
鍍金料號:11NR6-403025-92R

A_VDDPS5

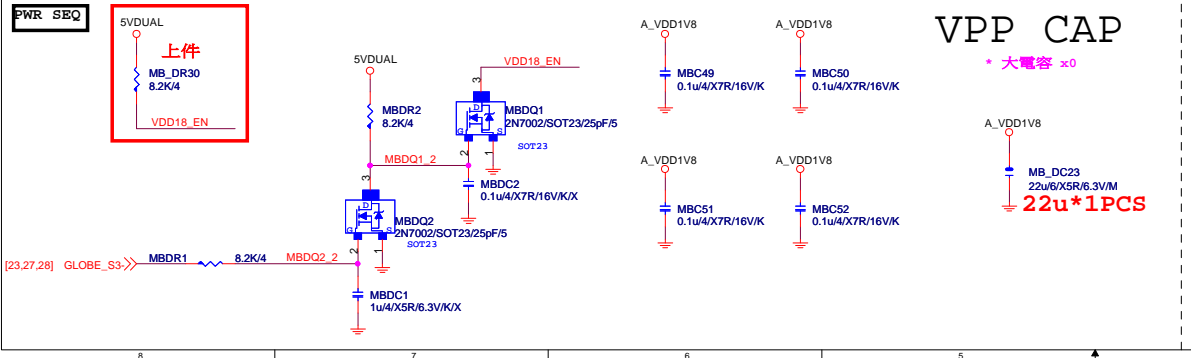


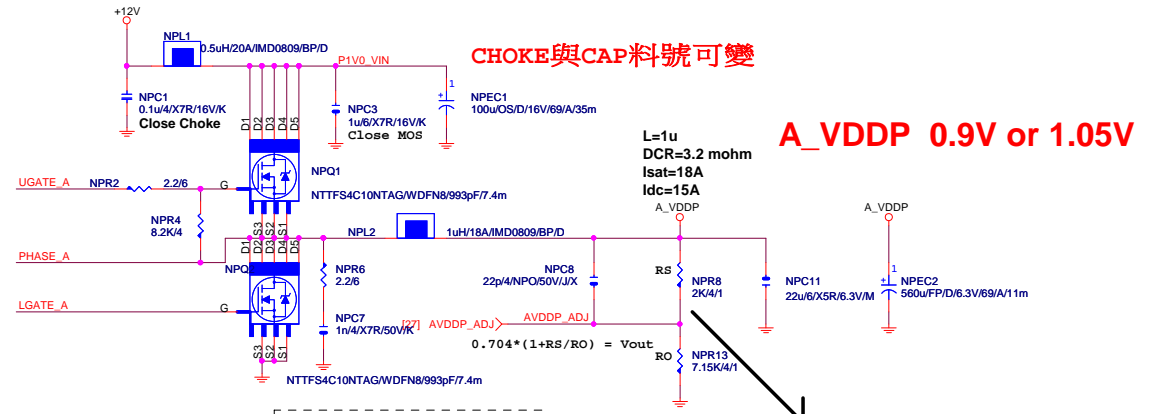
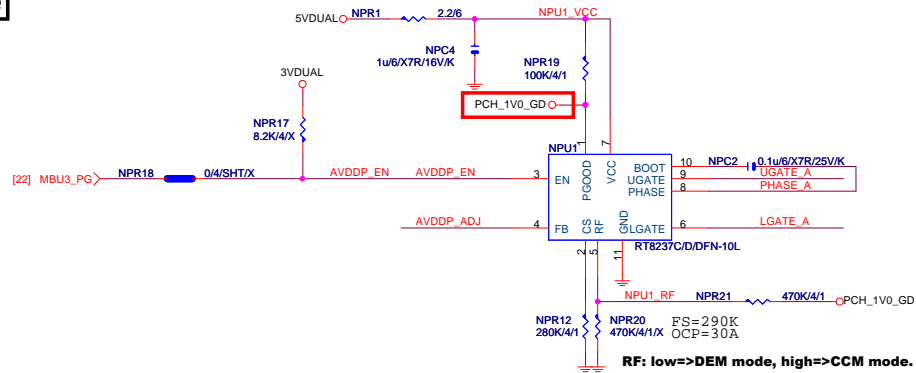
REV:0.4

A_VDD1V8



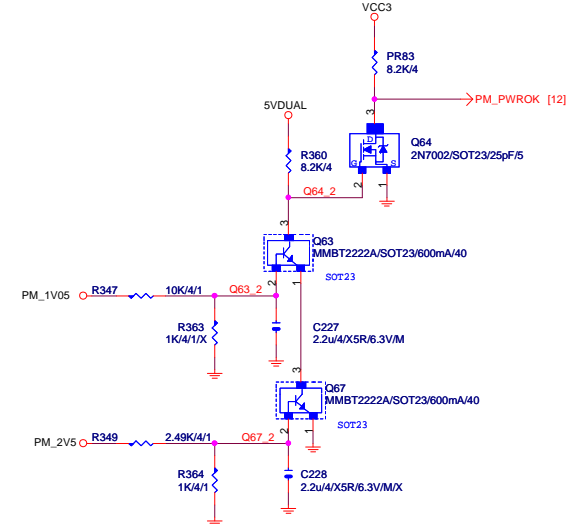
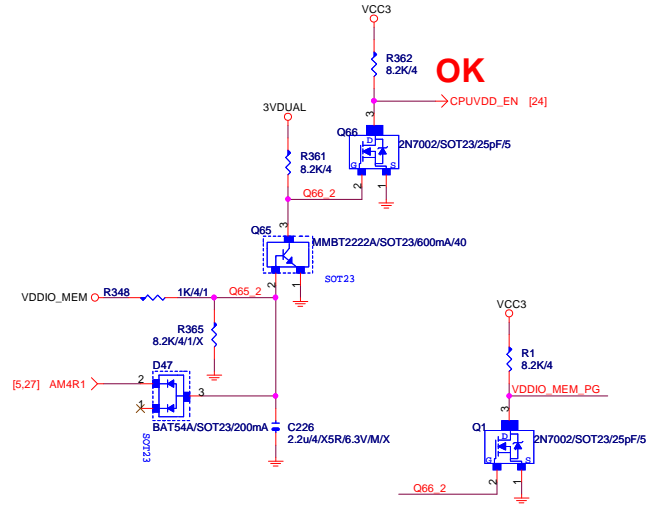
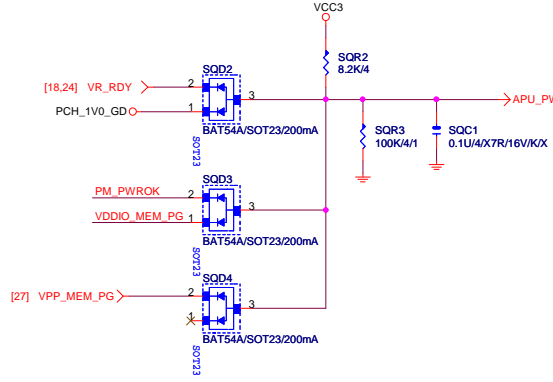
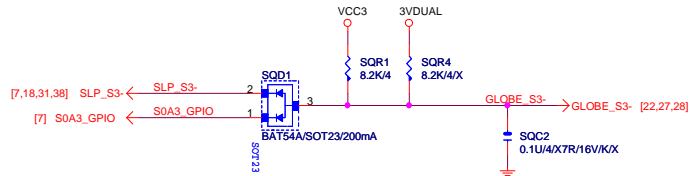
PWR SEQ

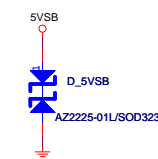
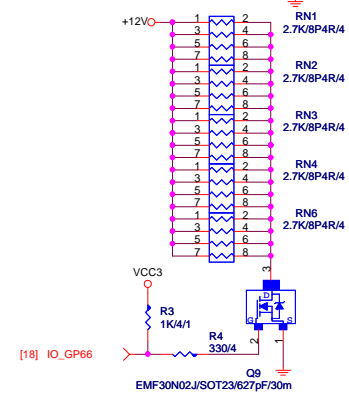
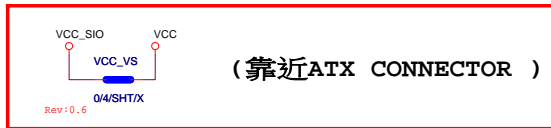
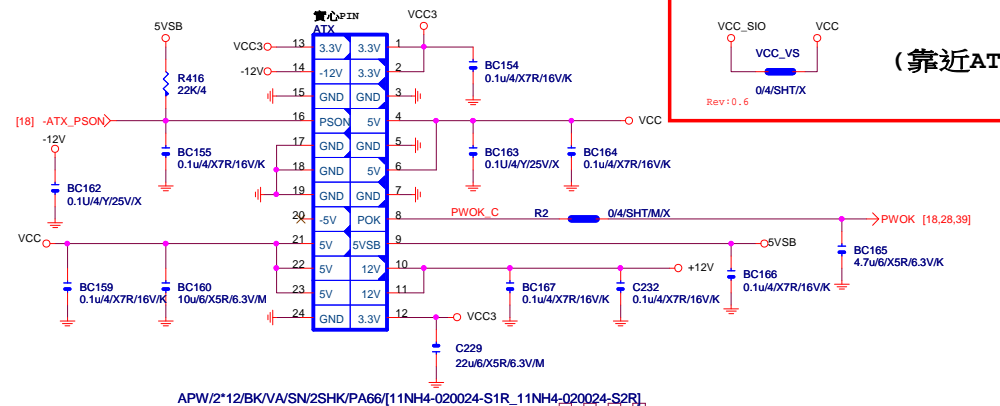
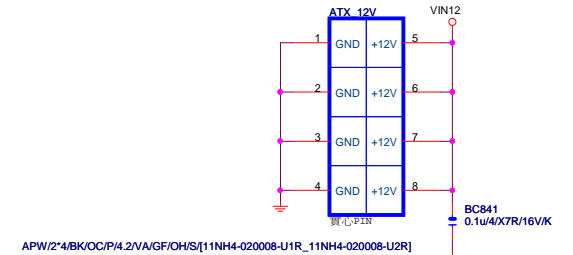
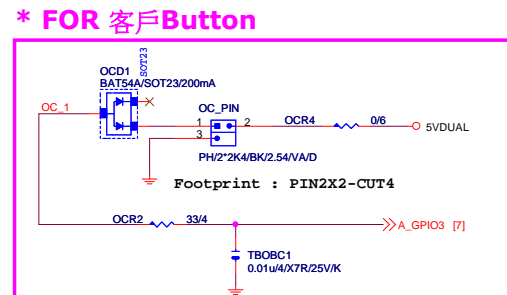
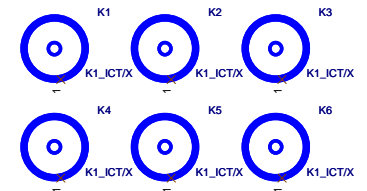
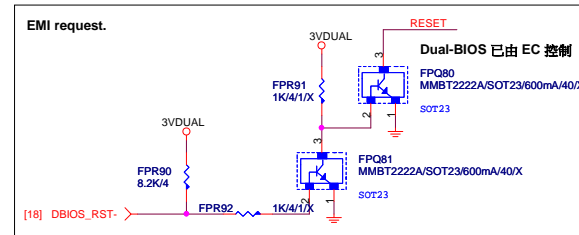
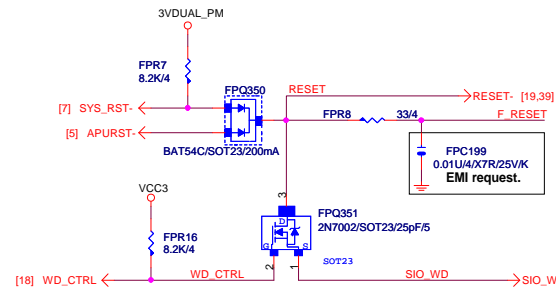




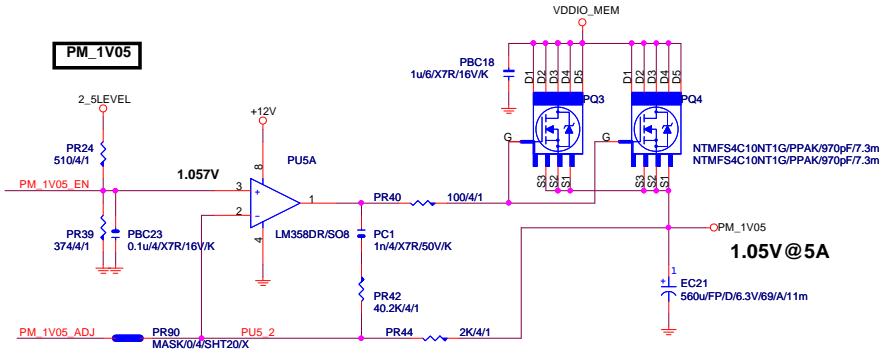
請放置CHOKE一出來的地方

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

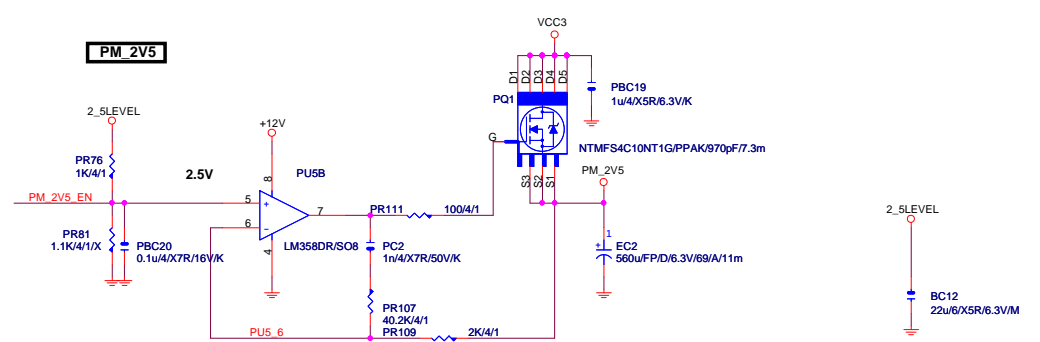




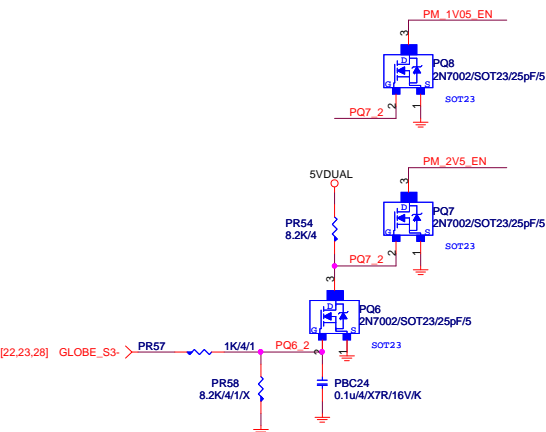
PM_1V05



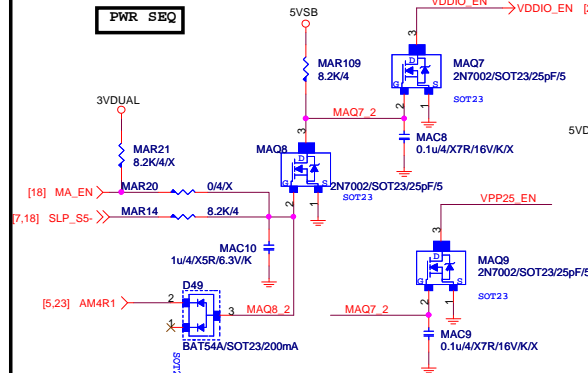
PM_2V5



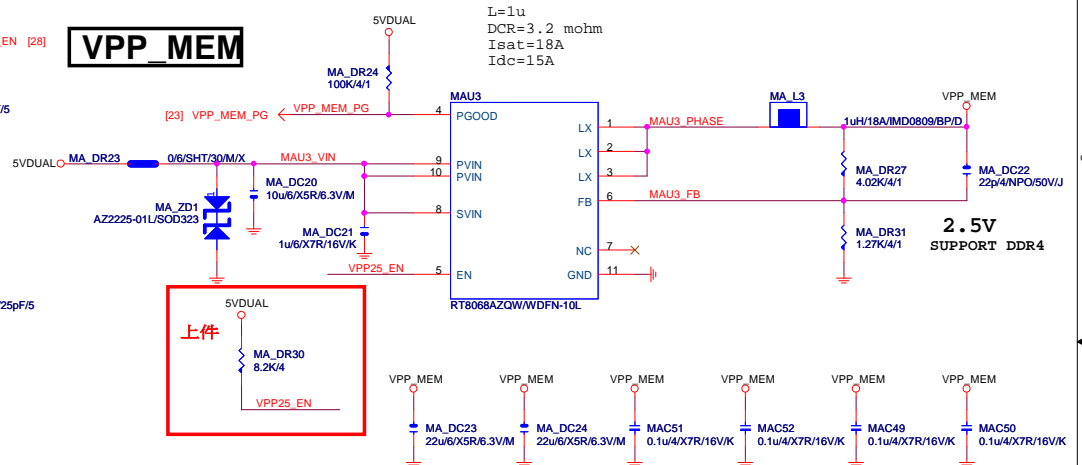
PWR_SEQ



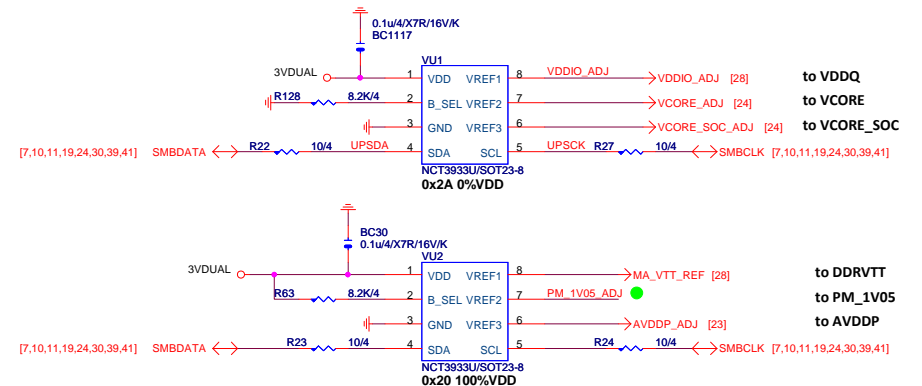
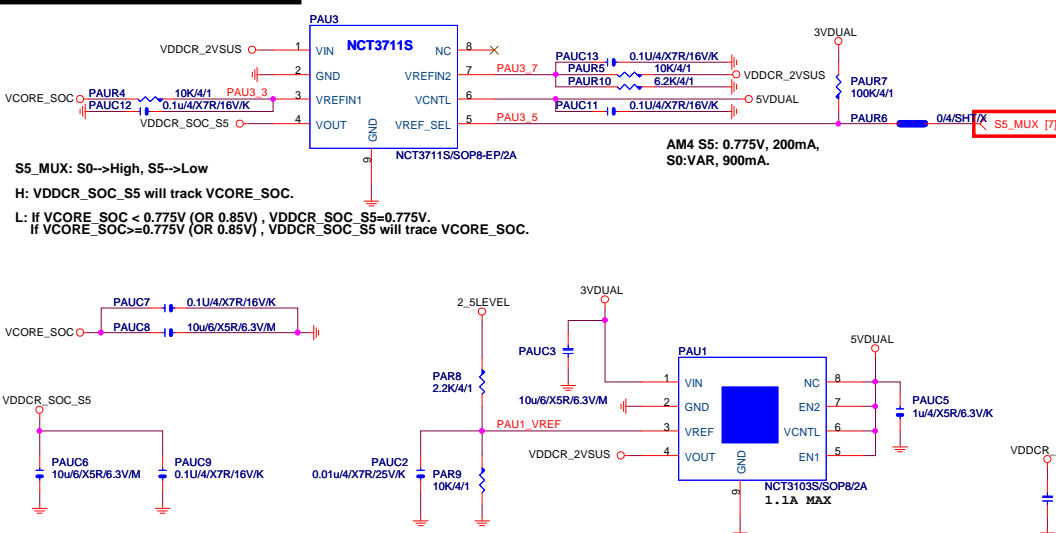
PWR_SEQ



VPP_MEM

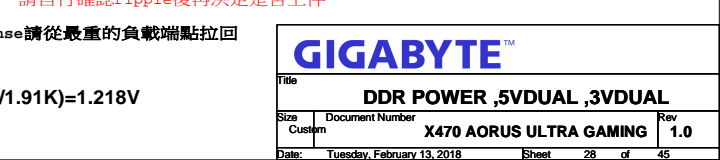
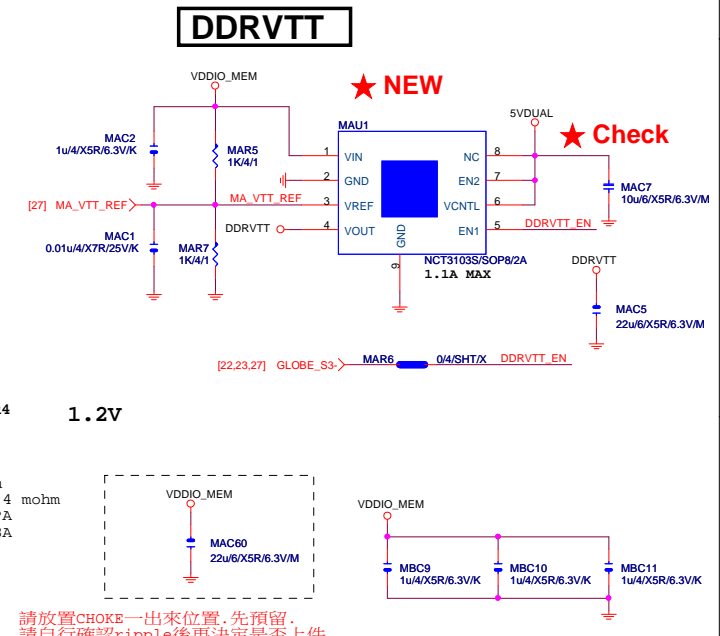
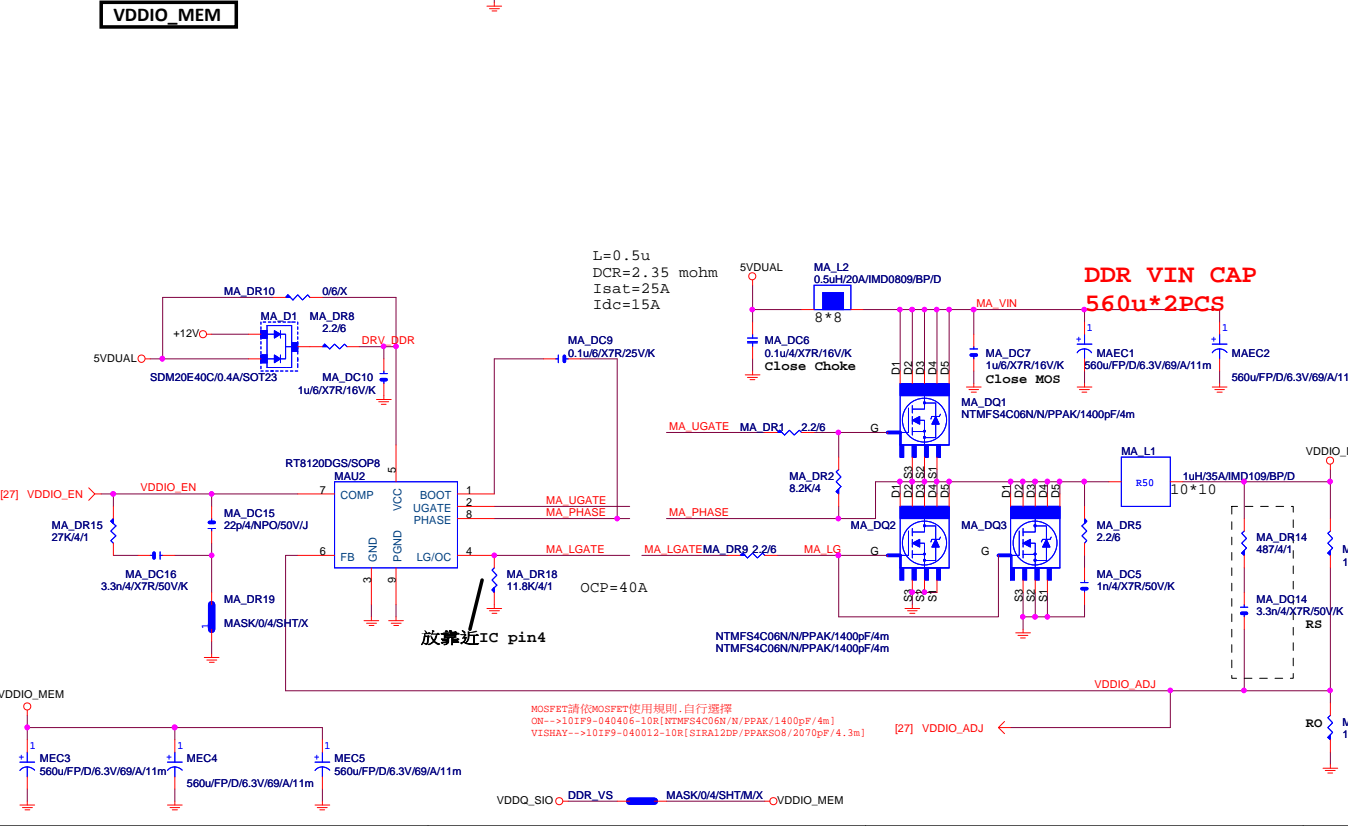
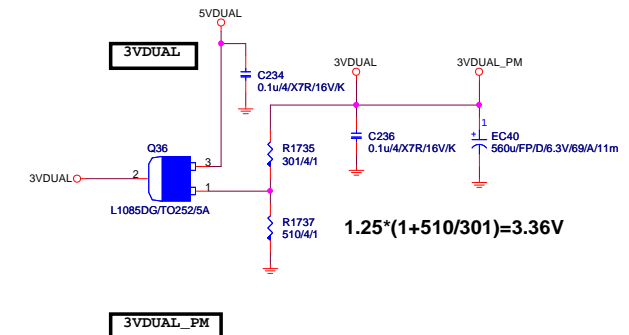
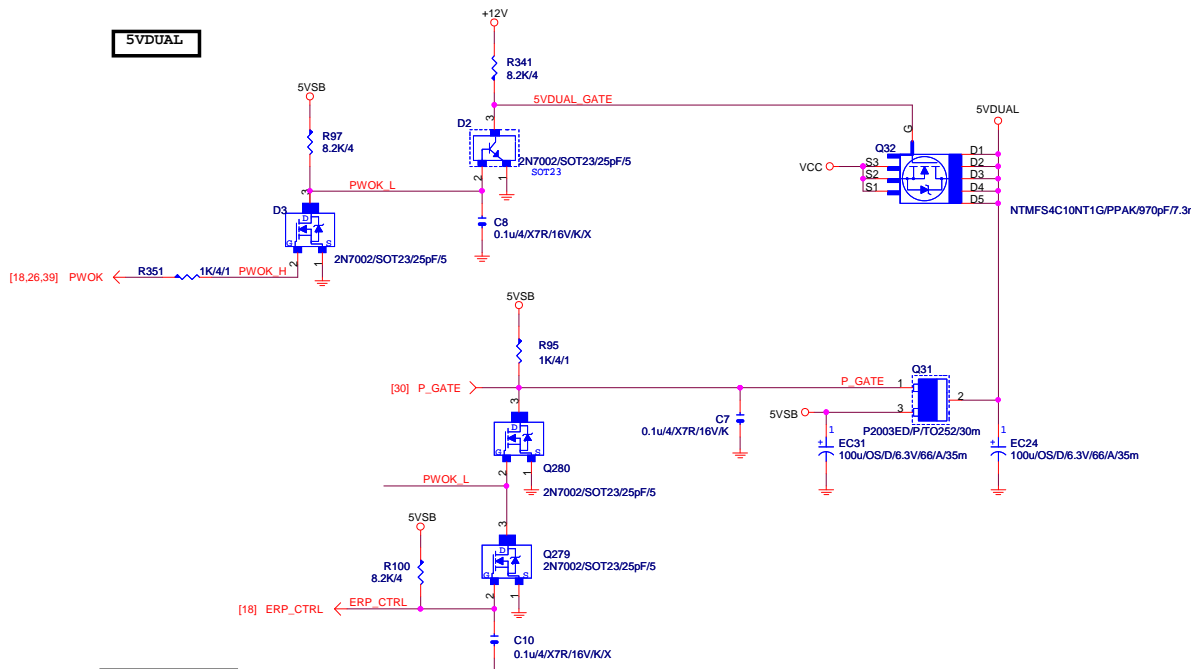


VDDCR SOC S5



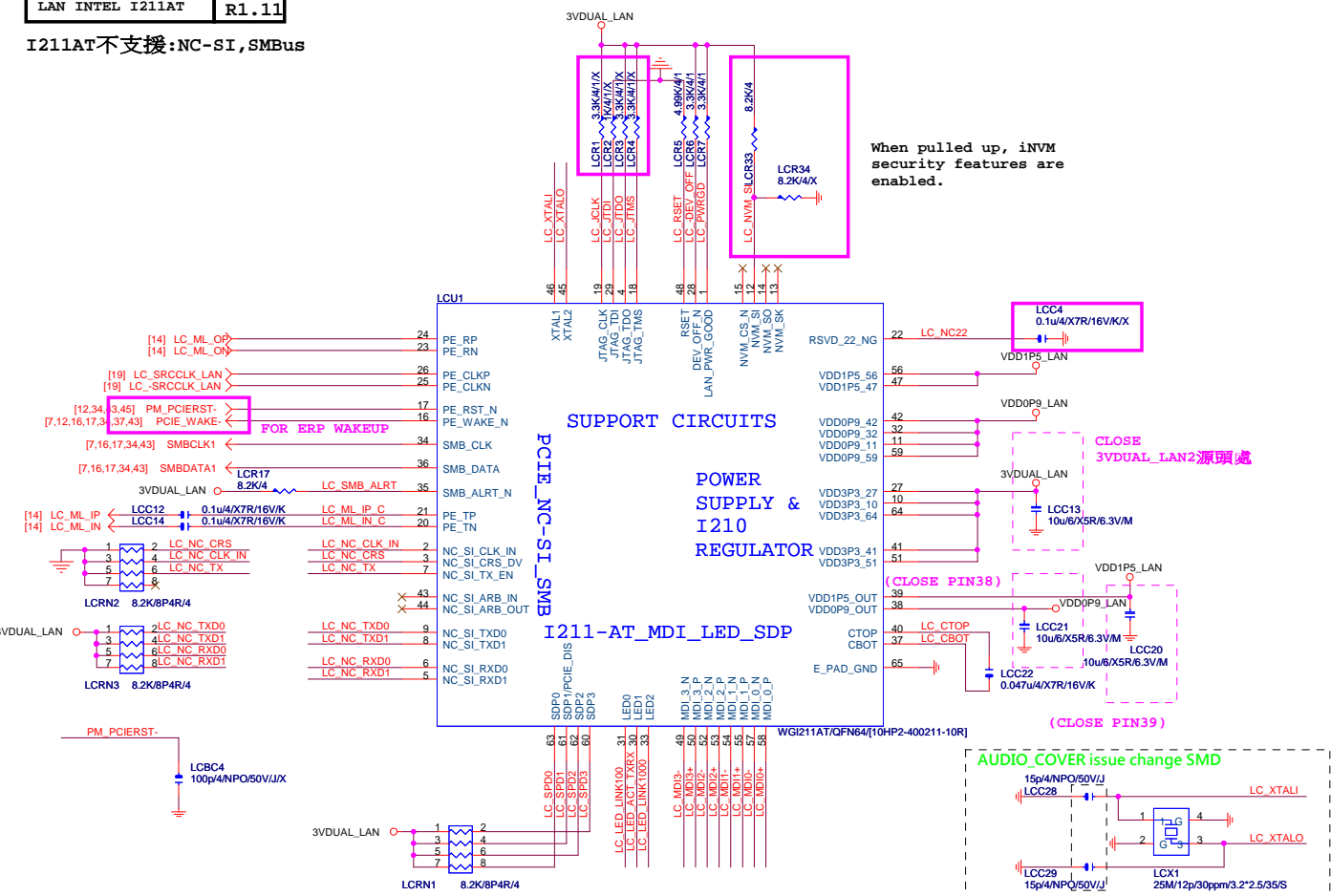
GIGABYTE

Title		
PM PWR,VPP_MEM,VDDCR_SOC_S5		
Size	Document Number	Rev
Custom	X470 AORUS ULTRA GAMING	1.0
Date:	Tuesday, February 13, 2018	Sheet 27 of 45

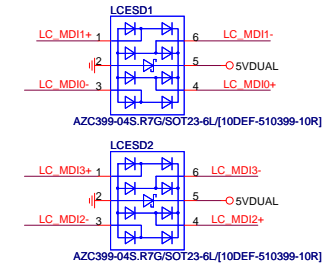


GIGABYTE™			
Title			
DDR POWER ,5VDUAL ,3VDUAL			
Size	Document Number	Rev	
Custom	X470 AORUS ULTRA GAMING	1.0	
Date:	Tuesday, February 13, 2018	Sheet	28 of 45

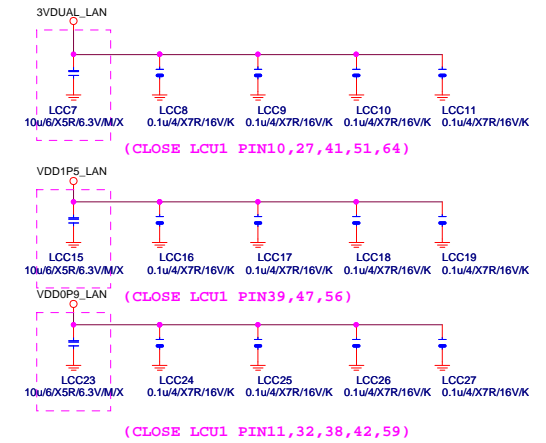
I211AT不支援:NC-SI,SMBus



LAN_COVER FOOT PRINT:LAN_COVER
MDI ESD 可變
[視SPEC需求]



LAN POWER



LAN POWER

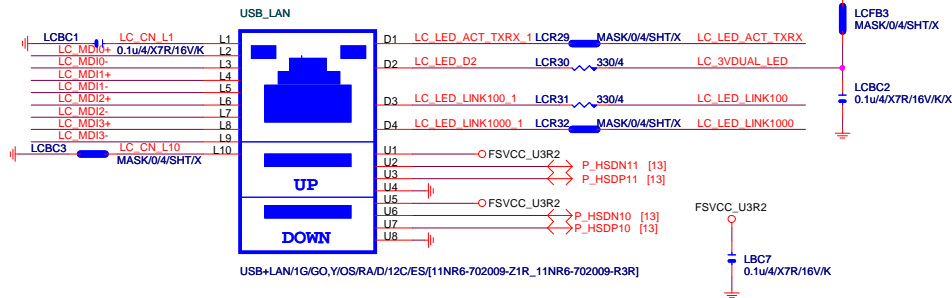


EMI SHORT PAD

USB_LAN

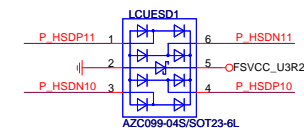
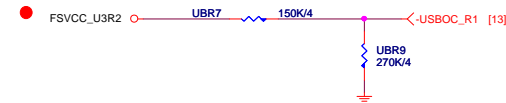
USB_LAN CONNECTOR note:可變更USB NAME

[I211]

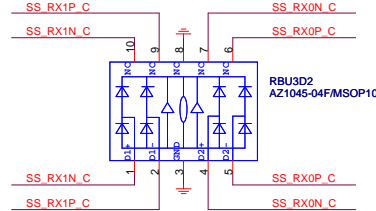
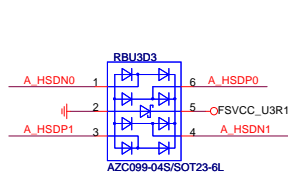
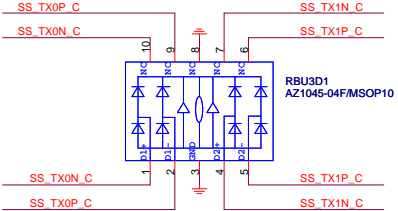
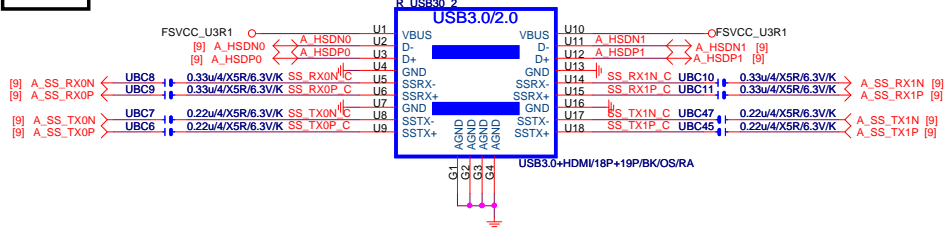


LA_MDI-->100歐姆:[20/4/8/4/20]

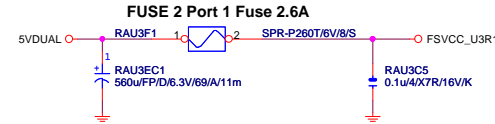
LA_MDI-->100歐姆:[20/4/8/4/20]



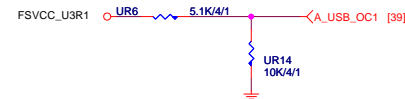
R_USB30



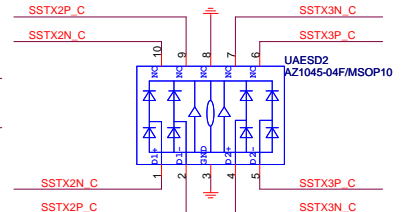
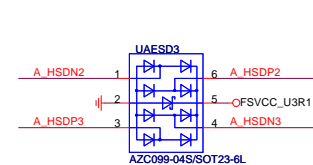
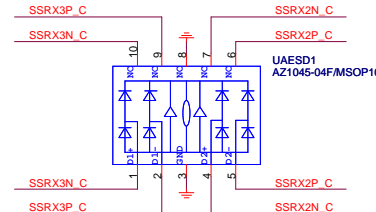
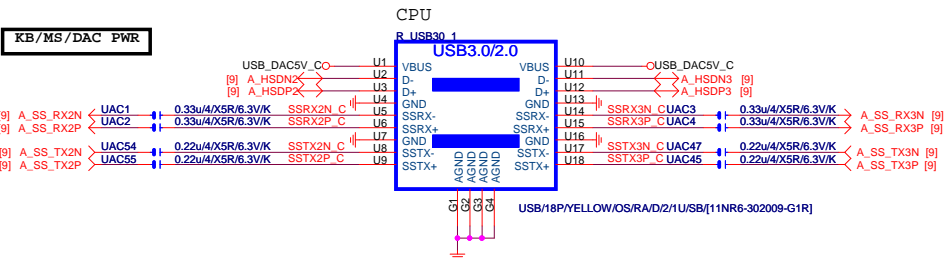
Close to connector



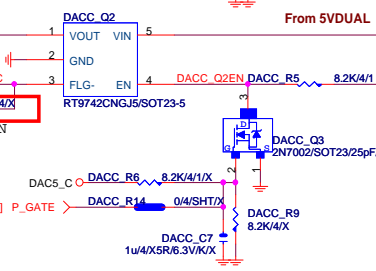
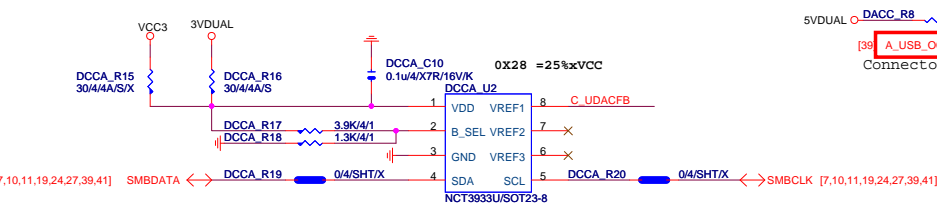
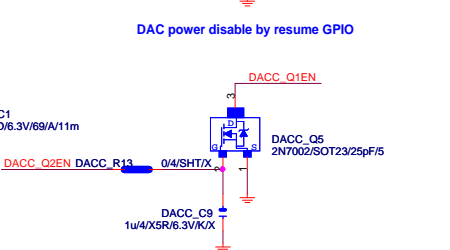
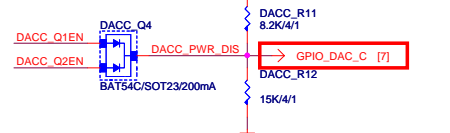
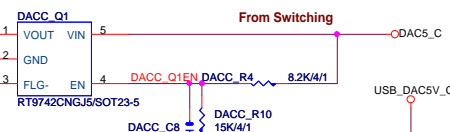
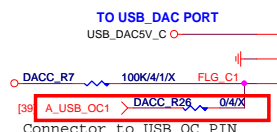
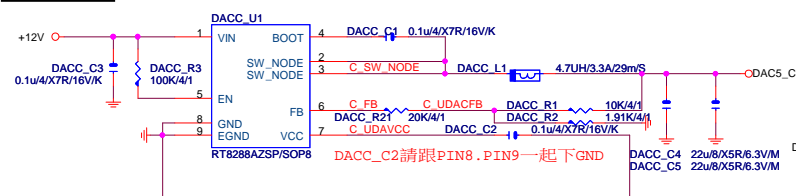
CPU OC



KB/MS/DAC PWR

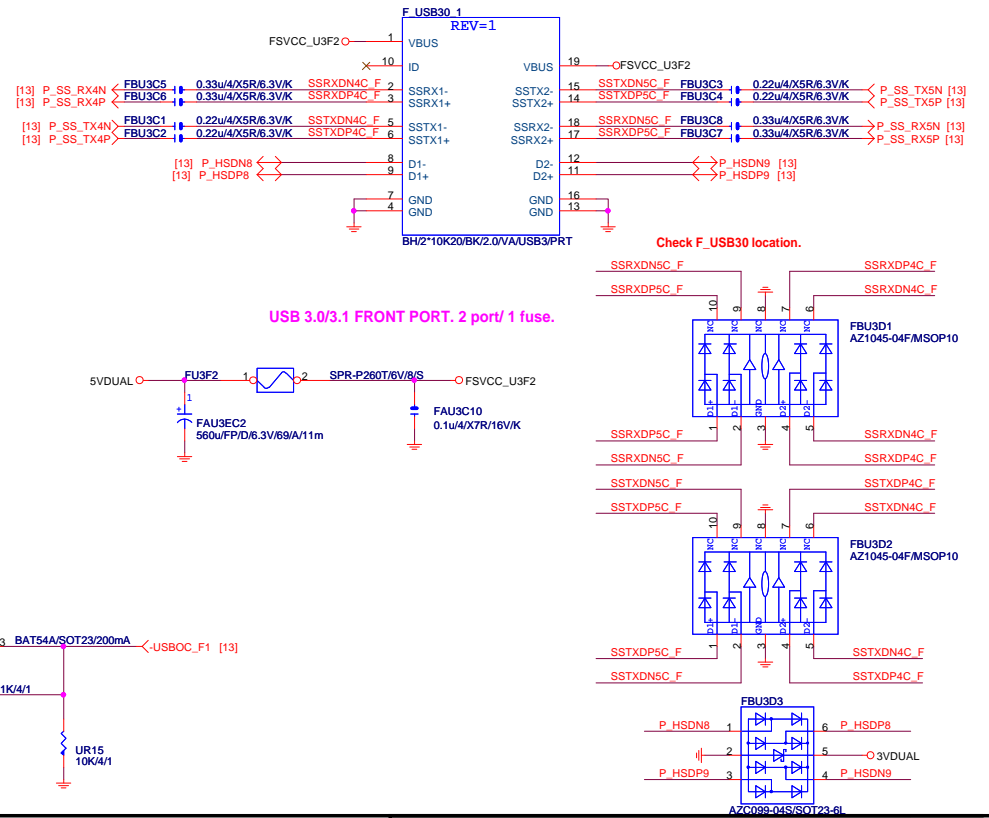
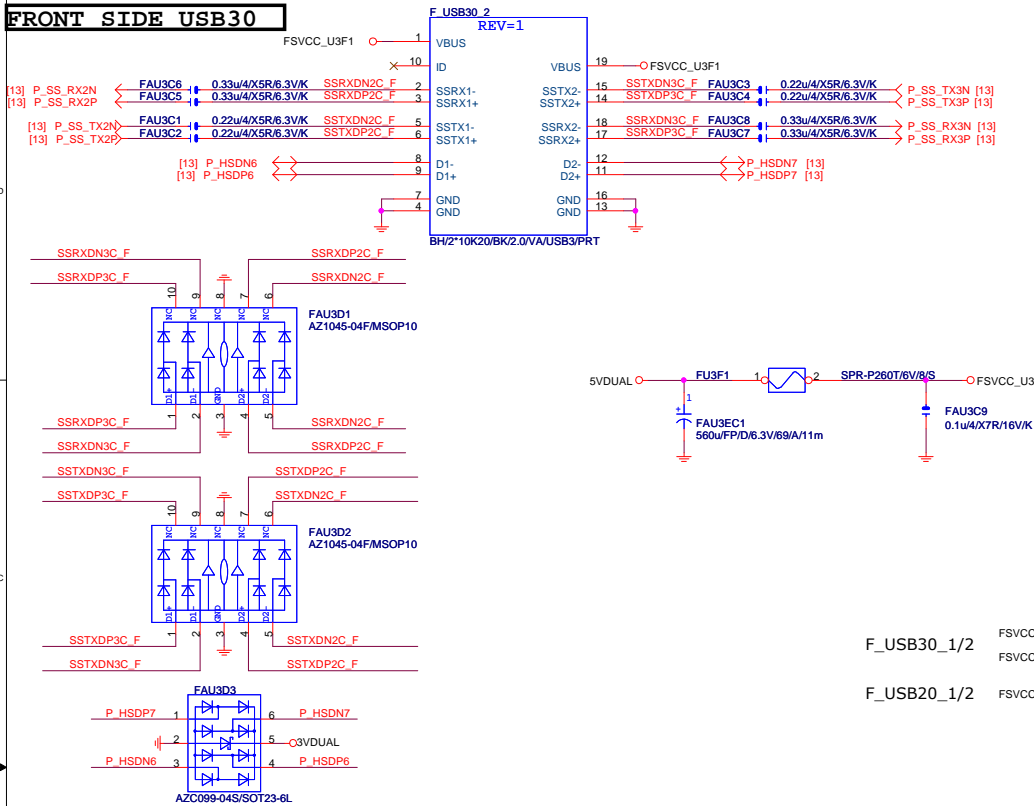
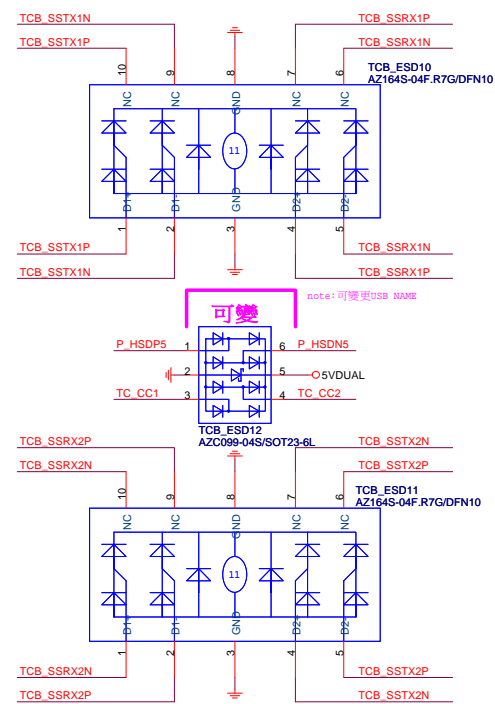
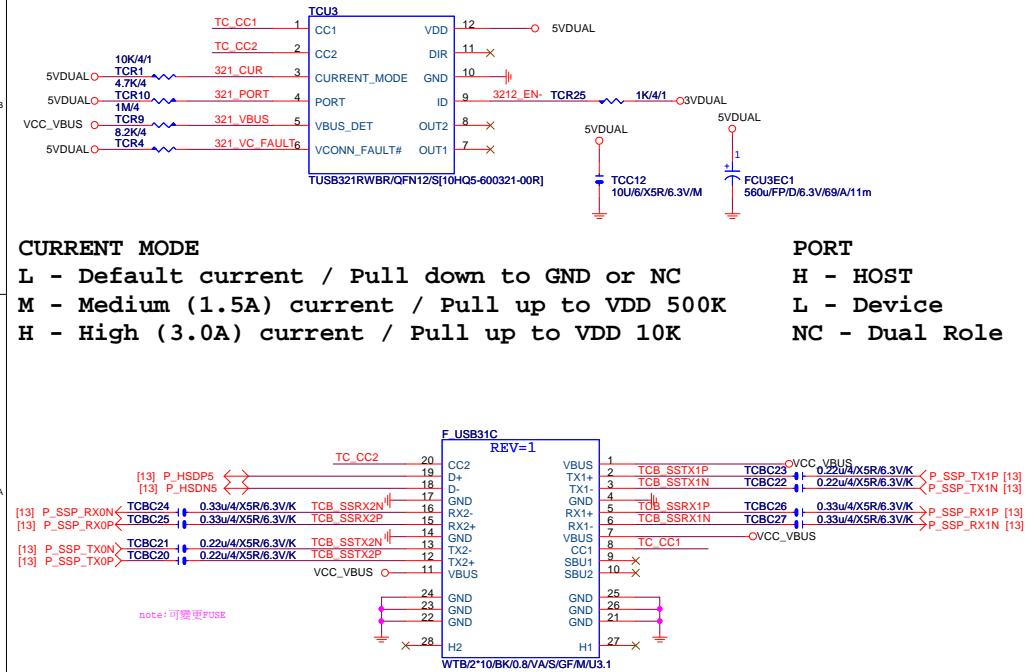


USB_DAC_C REV:0.13

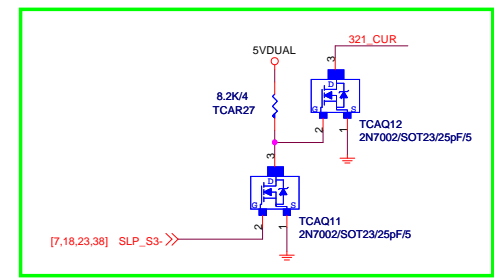
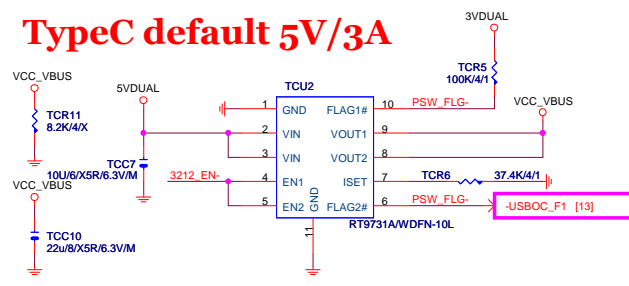


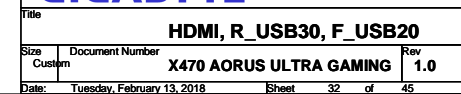
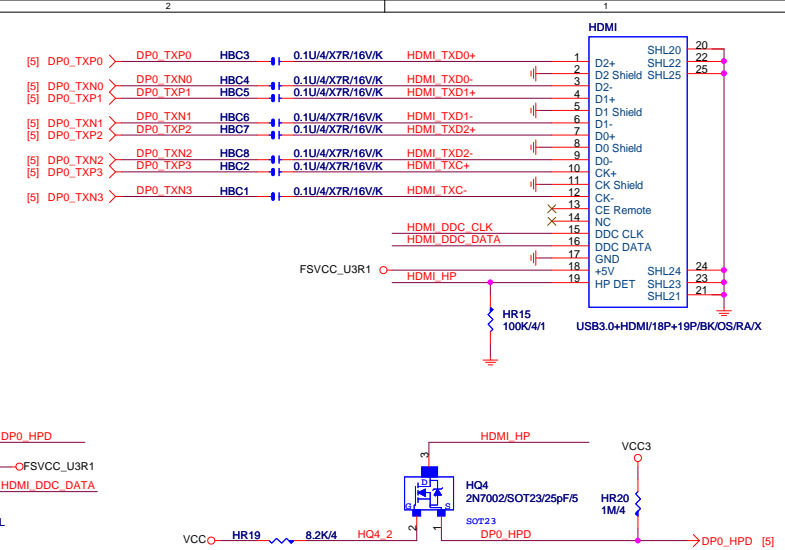
GIGABYTE™			
Title			
KB_MS_USB30			
Size	Document Number	Rev	
Custom	X470 AORUS ULTRA GAMING	1.0	
Date:	Tuesday, February 13, 2018	Sheet	30 of 45

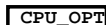
FRONT SIDE USB30

**Front U31 w/ TI HD3SS3220**

TypeC default 5V/3A







請選擇適用的USBport：
SOC/UD7/UD5/G1/G7：USB4
;UD3/G5:USB6

NET 可變

[13] P_HSDP0
[13] P_HSDN0

PCIe:15/4/4/15(breakout min 8/4/4/8)
外層Impedance=85 ± 17.5%

PCIe:15/4/4/15(breakout min 8/4/4/8)
內層 Impedance=85 ± 12%

NET 可變

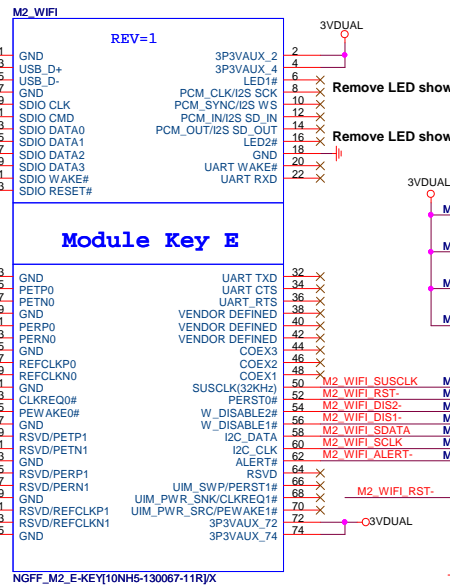
WIFI use PCIe port4 in X99

MASK/0.1u/4/X7R/16V/K/X
M2W4
M2WCS
MASK/0.1u/4/X7R/16V/K/X

[14] GPP_TXP2
[14] GPP_TXN2
[14] M2_WIFI_IP
[14] M2_WIFI_IN
[19] CK_WIFI_100M_DP
[19] CK_WIFI_100M_DN

M2WR1
M2WR6
MASK/8.2K/4/X
0/4/SHT/20/X
WIFI CKREQ-
WIFI WAKE-

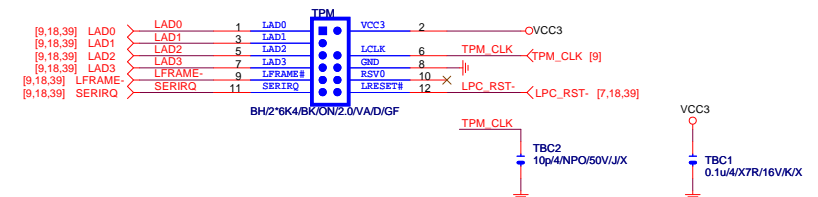
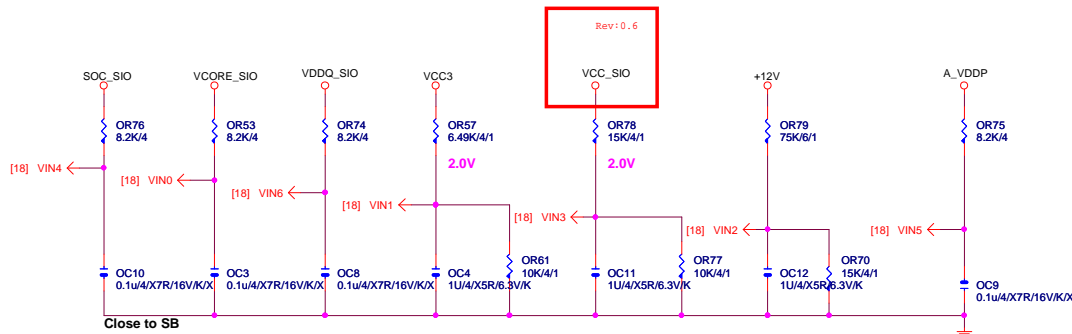
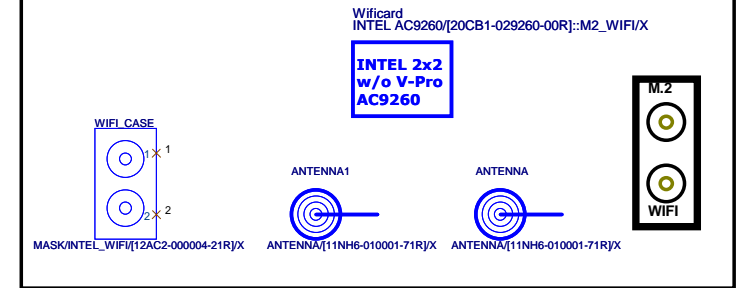
WIFI CKREQL connect to relative pin.



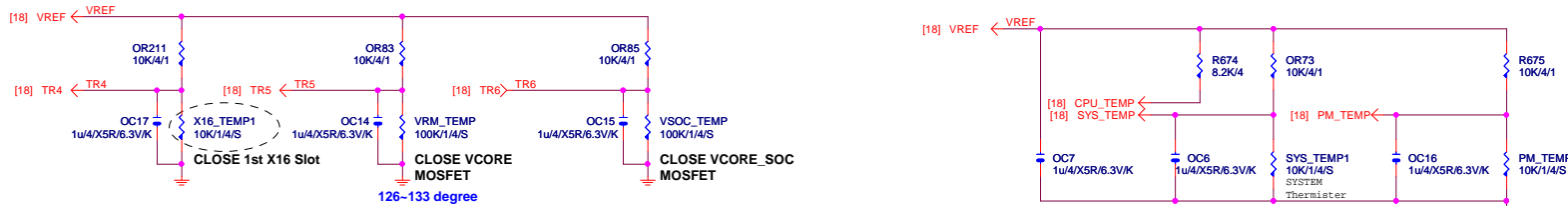
★Update 2015-02-11

FOR M.2 WIFI MODULE @ REAR PANEL

一套WIFI MODULE包含外框+WIFI CARD+天線



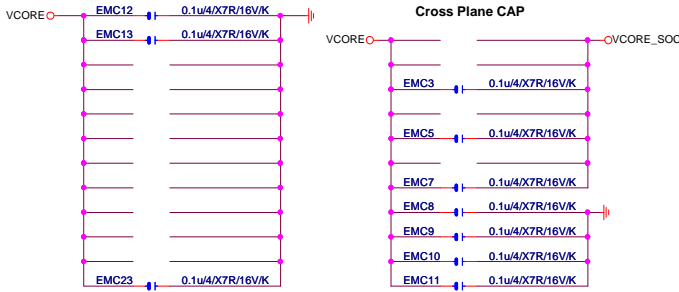
Hardware Monitor circuits



GIGABYTE™

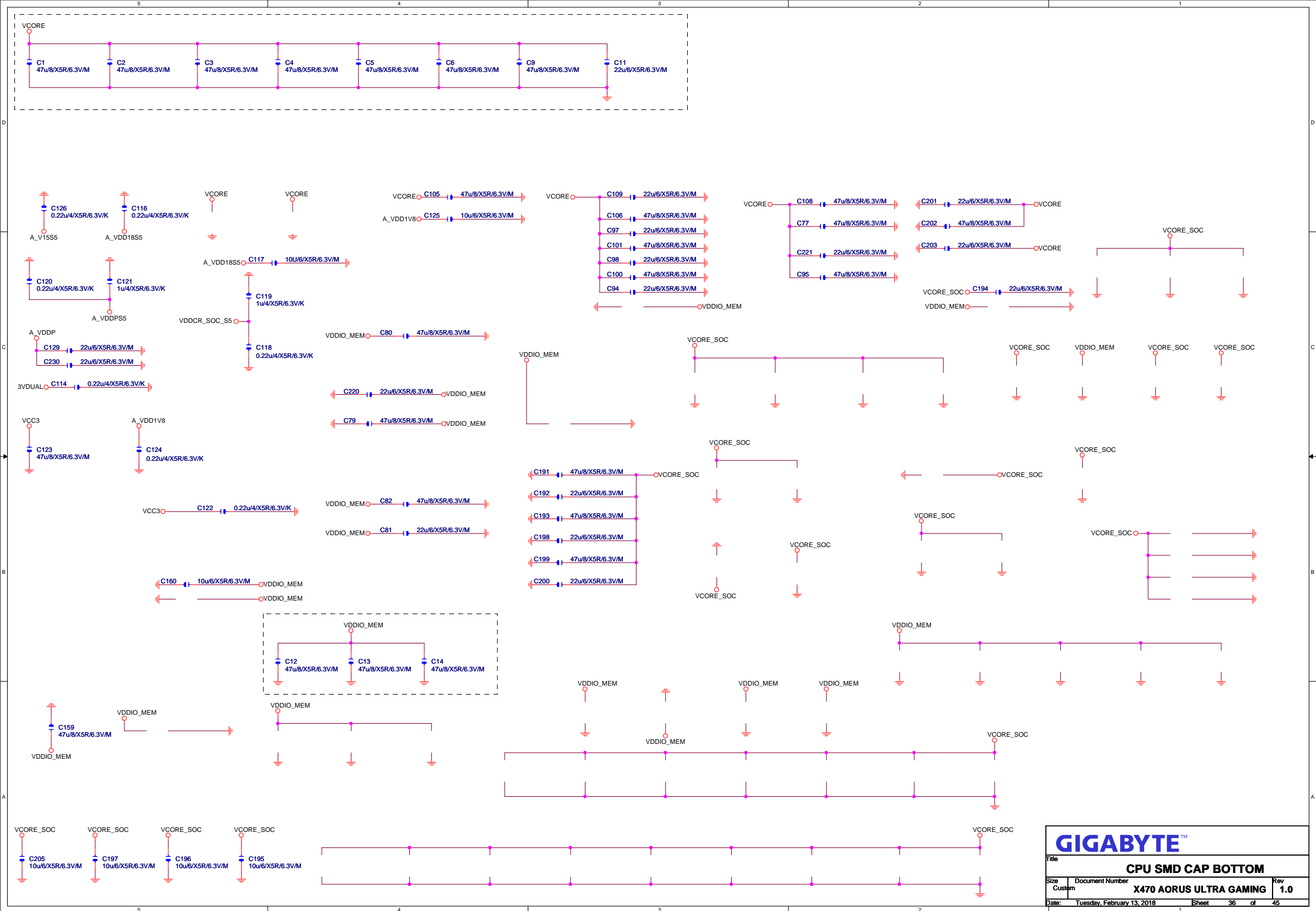
Title			
HWM, TPM, COM			
Size	Document Number	Rev	
Custom	X470 AORUS ULTRA GAMING	1.0	
Date:	Tuesday, February 13, 2018	Sheet	34 of 45

CPU TOP CAVITY



GIGABYTE™

Title			
CPU SMD CAP TOP			
Size	Document Number	Rev	
Custom	X470 AORUS ULTRA GAMING	1.0	
Date:	Tuesday, February 13, 2018	Sheet	35 of 45



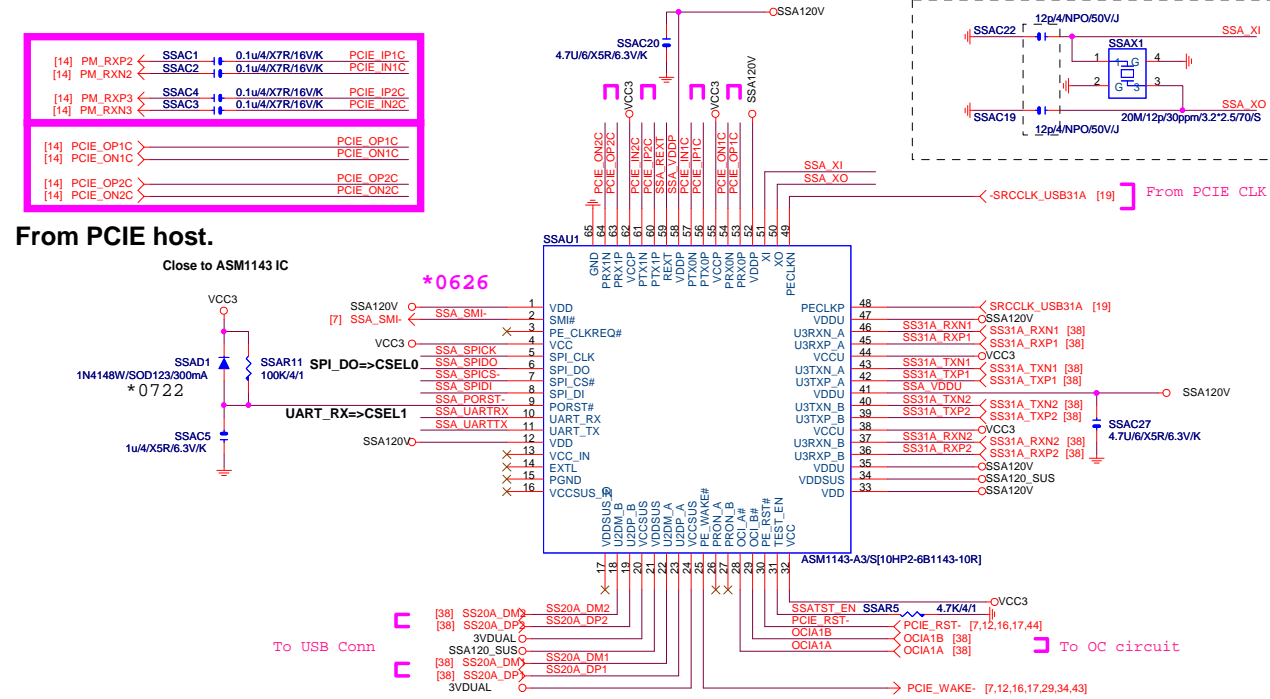
ASM1143 USB3 Host Rev0.63
PCIE Gen3 X1 or PCIE Gen2 X2
To PCIE host.

Color markers can be changed by model

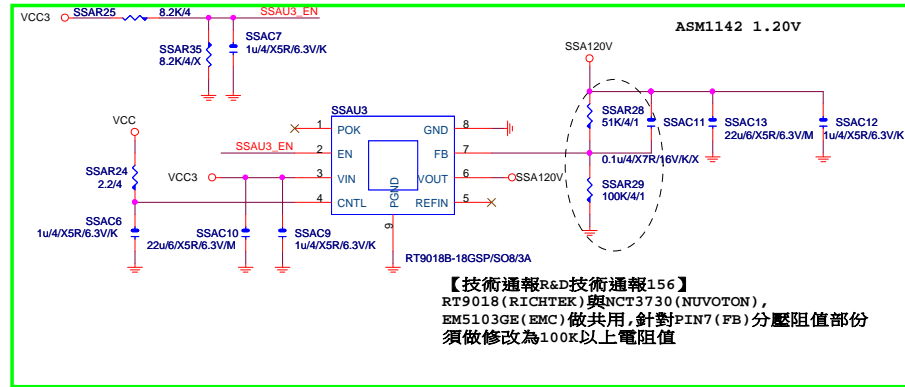
ASM1143 USB3.1

Base on ASM1142 0.3 Reference SCH

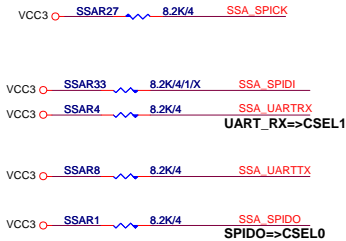
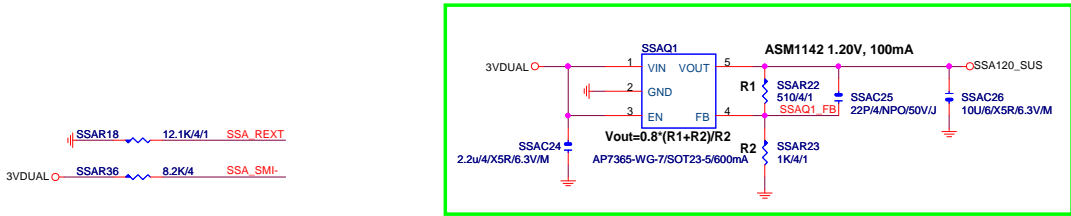
From PCIE host.



To USB Conn



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
須做修改為 100K 以上電阻值



CSEL1	CSEL0	
1	1	External 20MHz Crystal (Asynchronous)
0	1	48MHz clock input (Synchronous)
X	0	Reserved for Test

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Title

ASM1143 USB31

Size

Custom

Document Number

X470 AORUS ULTRA GAMING

Rev

1.0

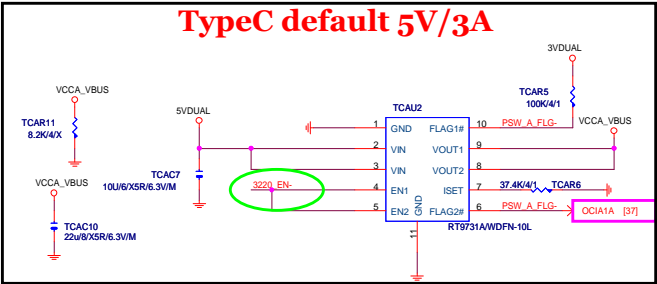
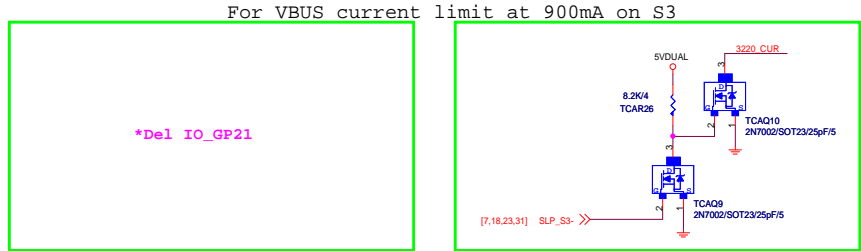
Date

Tuesday, February 13, 2018

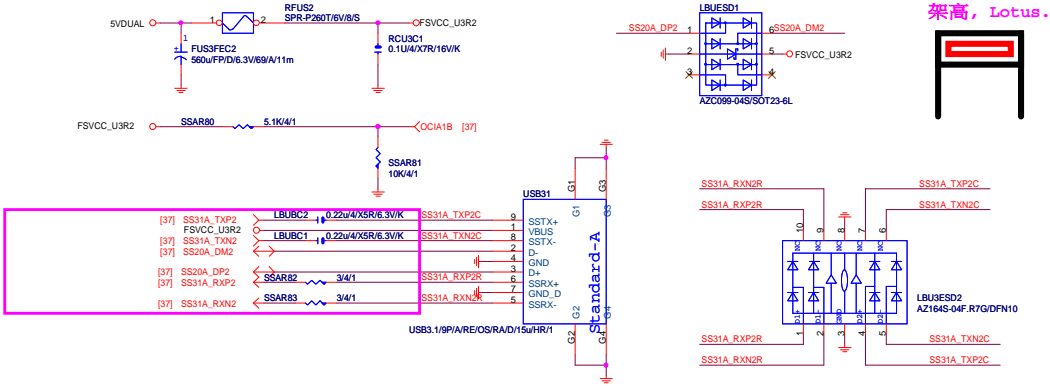
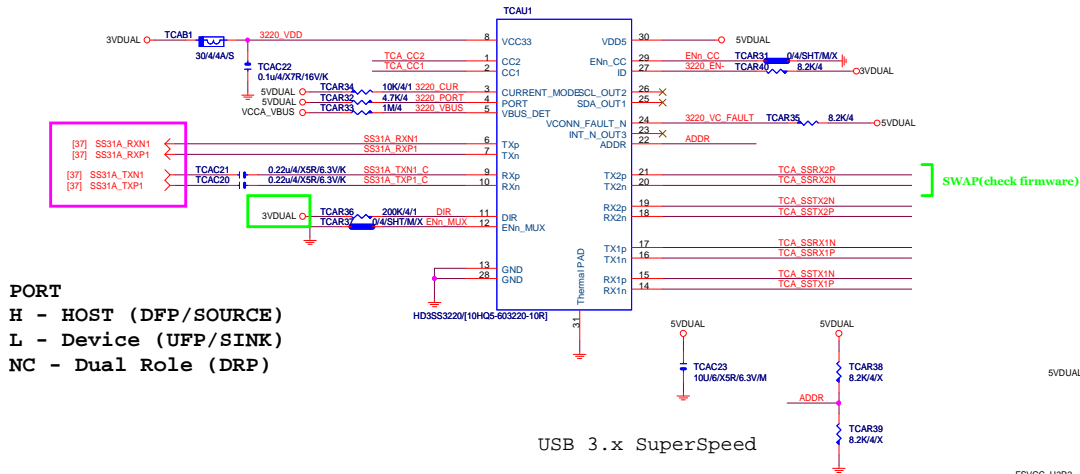
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ASM2142 USB31 Host Rev0.3
TI HD3SS3220



For USB3.1 TypeA SCH

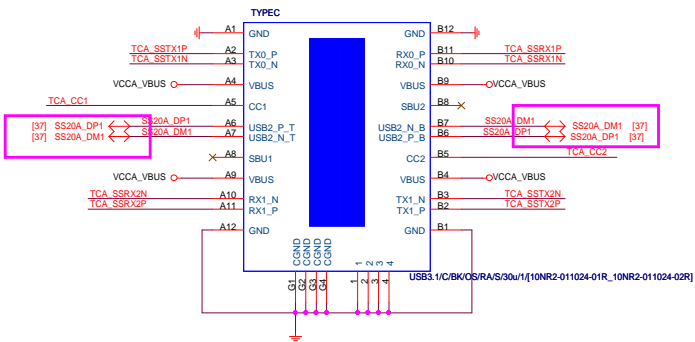


CURRENT MODE

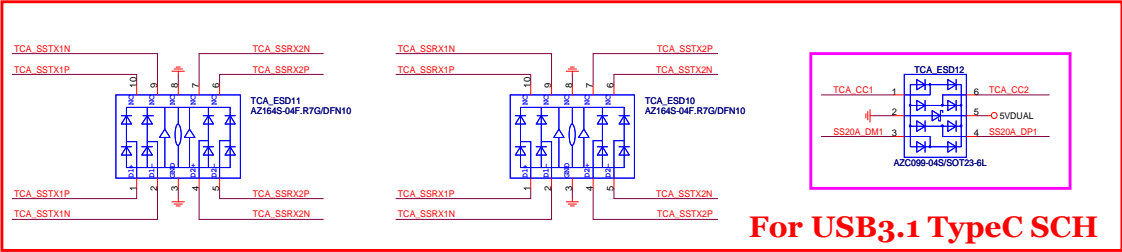
L - Default (900mA) / Pull down to GND or NC

M - Medium (1.5A) / Pull up to VDD 500K

H - High (3.0A) / Pull up to VDD 10K



USB2.0 can be used the same source

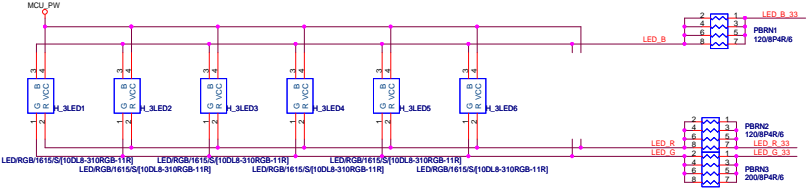


Color markers can be changed by model

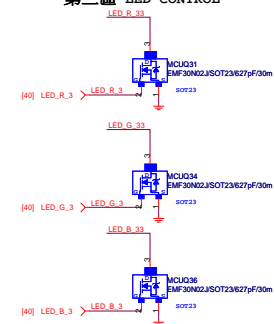
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TI HD3SS3220		
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第三區 LED

FOR PCH 正發光 LED*4 (位置在正板,依據PCH_HS設計擺放)



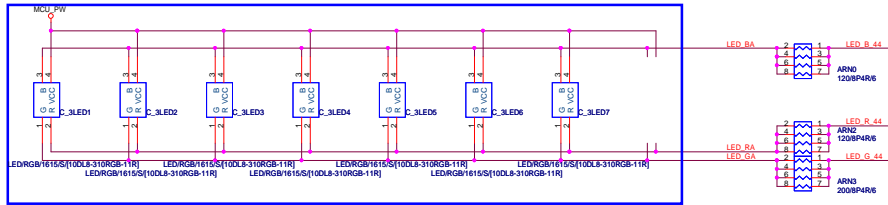
第三區 LED CONTROL



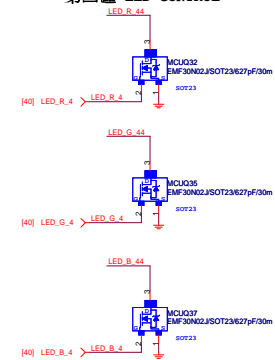
RGB LED壓克力燈條 REMOVE

第四區 LED

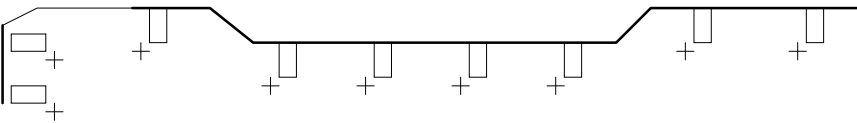
FOR AUDIO 正發光 LED*7 C_3LED1~7)



第四區 LED CONTROL

FOR PCIEX16_1 側發光 LED*4
(位置在PCIEX16_1 SLOT兩側各4顆)FOR PCIEX8 側發光 LED*4
(位置在PCIEX8 SLOT兩側各4顆)

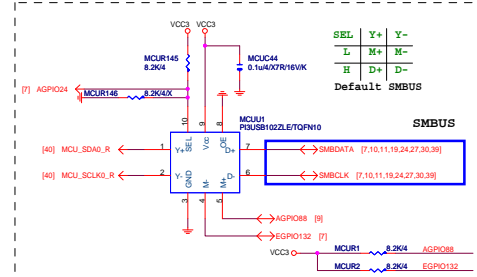
Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項：

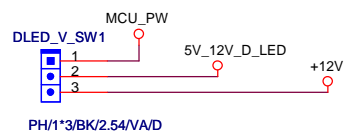
1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1, ECF2, ECF3, ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B, GPD0_SDA_BB, GPD0_SDA_C, GPD0_SDA_CC

For AMD MCU update



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第六區 LED（靠近左上板邊位置）



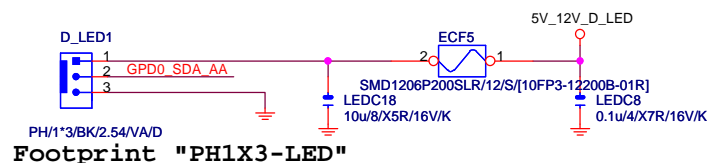
DLED_V_SW1



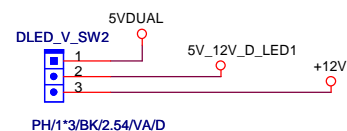
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

DLED_V_SW1	
1-2	5V
2-3	12V

Digital LED Strip1



第七區 LED（靠近右下DDR板邊位置）



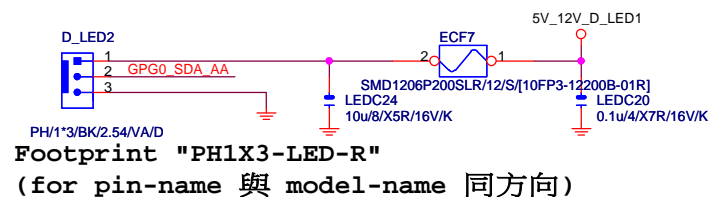
DLED_V_SW2



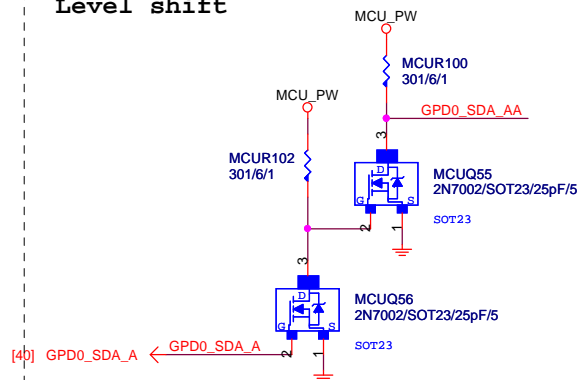
JP/1*2/BK/H/2.54/C/GF/[11NH1-000102-V1R]:[1-2]CLOSE

DLED_V_SW2	
1-2	5V
2-3	12V

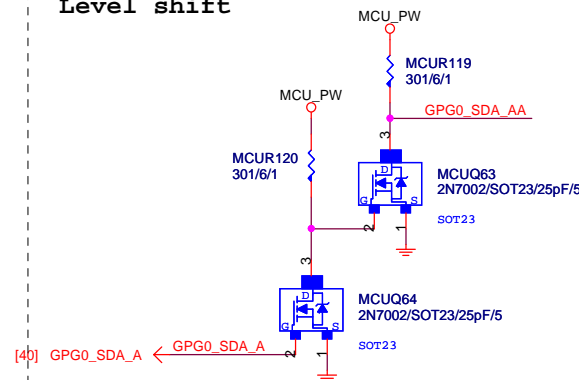
Digital LED Strip2



Level shift

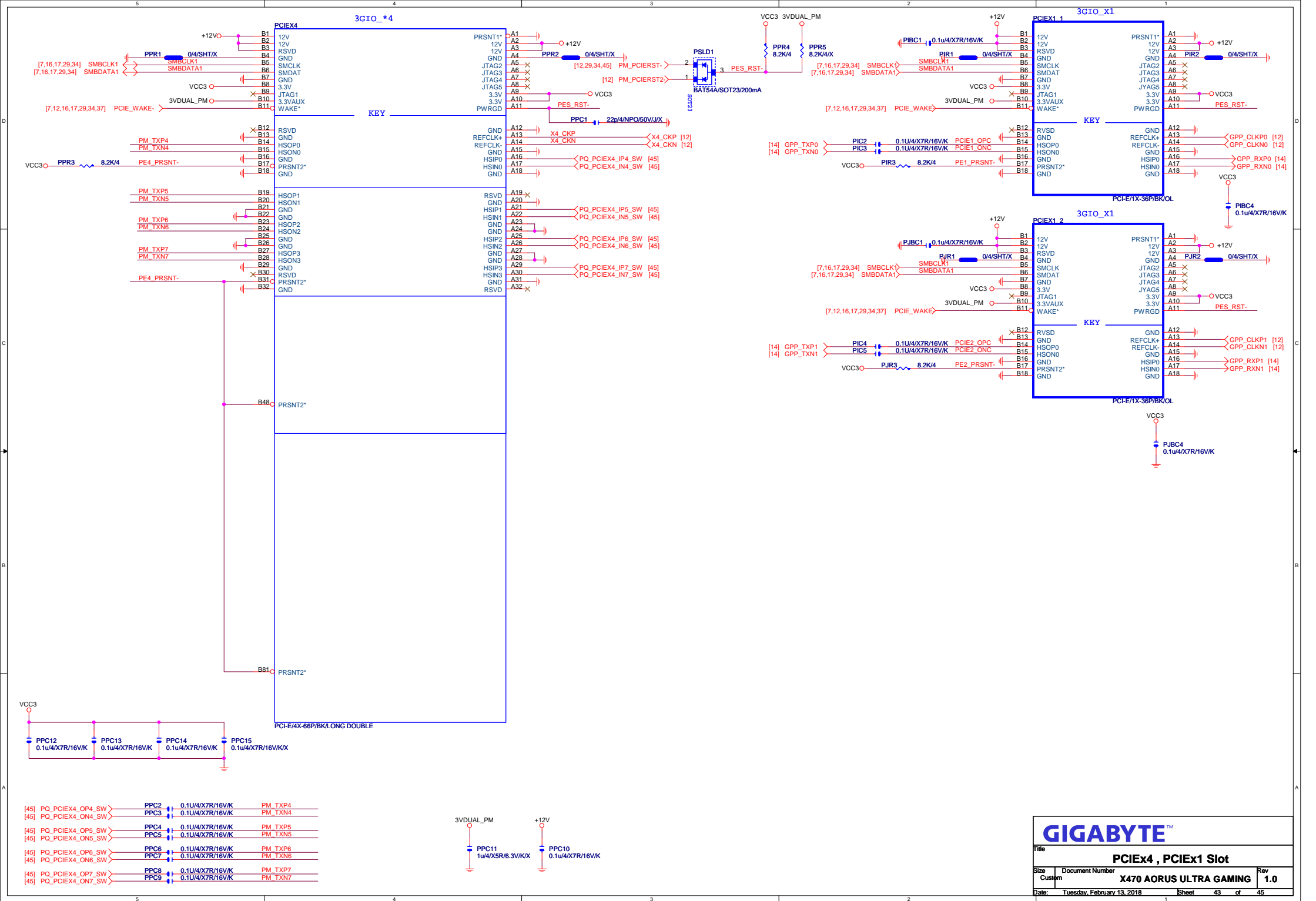


Level shift

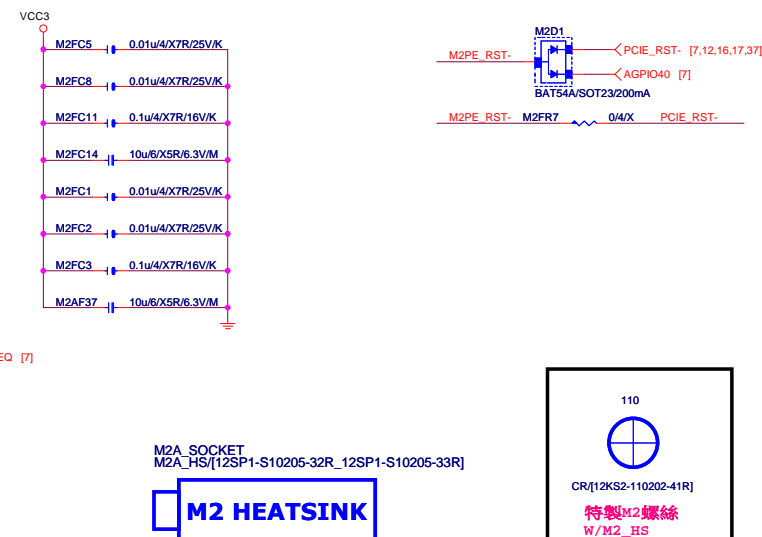
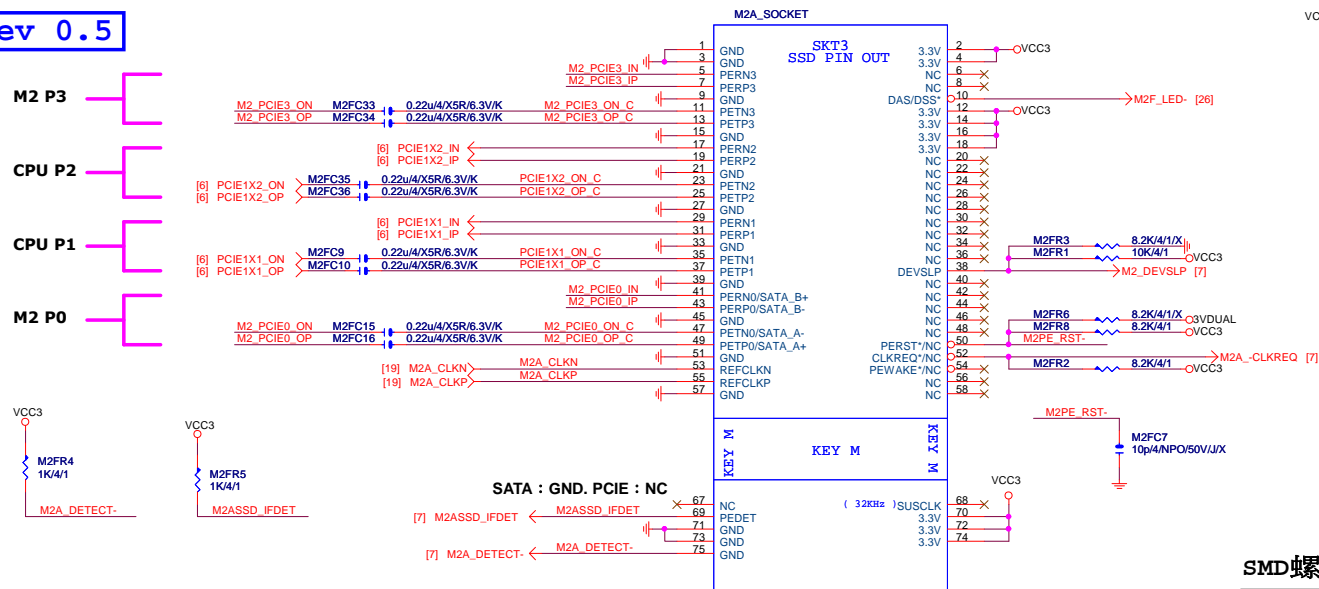


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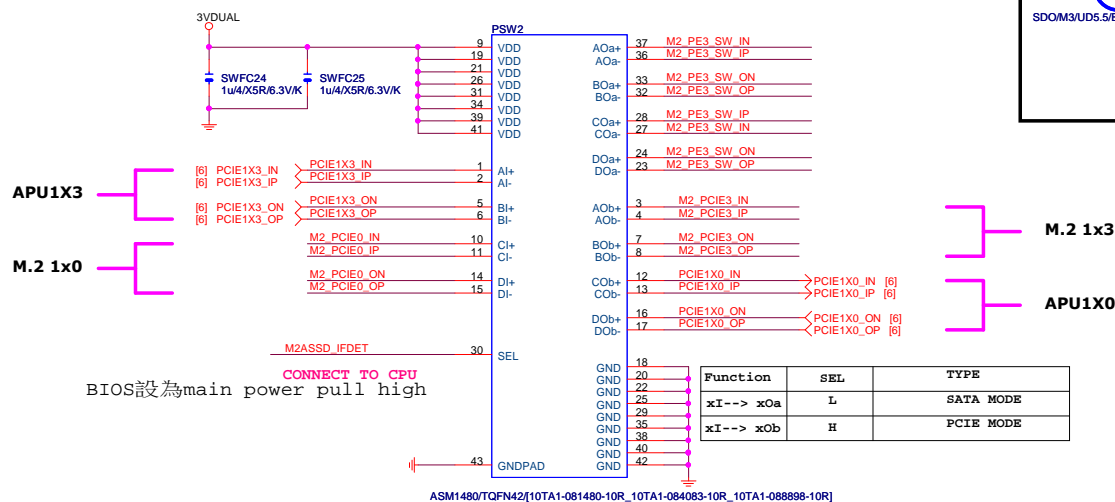
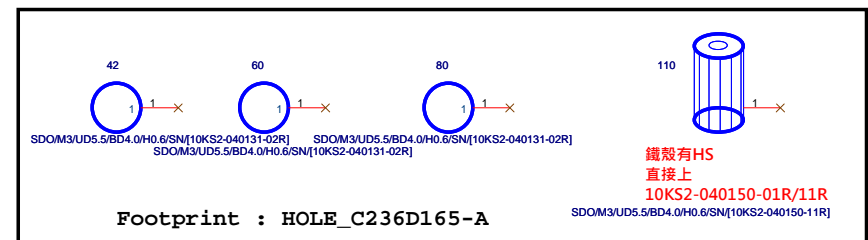
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D LED		
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Rev 0.5



SMD螺柱



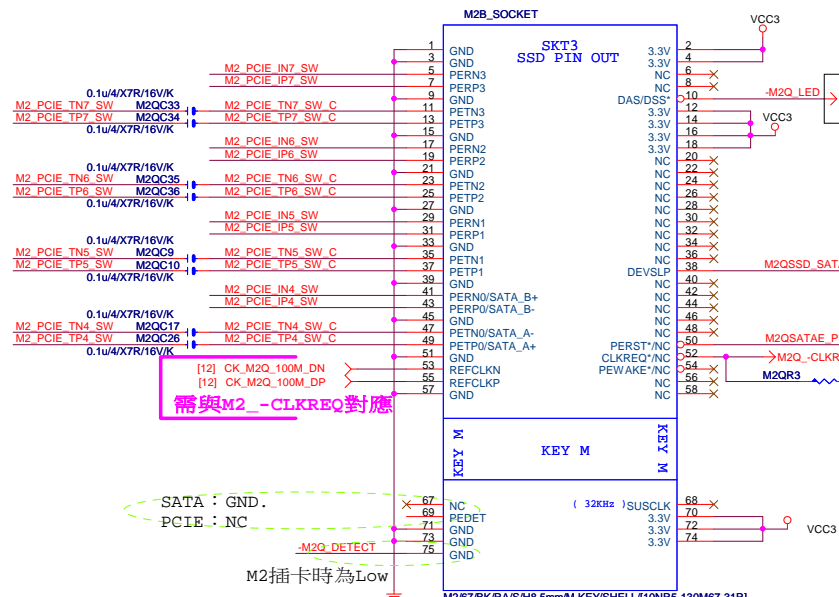
Rev 0.2

M.2 Lane4 from GPP7

M.2 Lane4 from GPP6

M.2 Lane4 from GPP5

M.2 Lane4 from GPP4



需與M2_-CLKREQ對應

SATA : GND.

PCI-E : NC

M2插卡時為Low

M.2 FOOTPRINT :M2_80

8.5H鐵殼 (第三代)

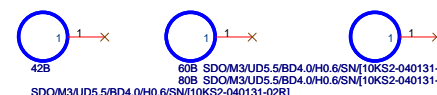
Footprint :M2_80(DIP)

轉接柱(十字溝)
架高

CR[12KSF-F10303-11R]

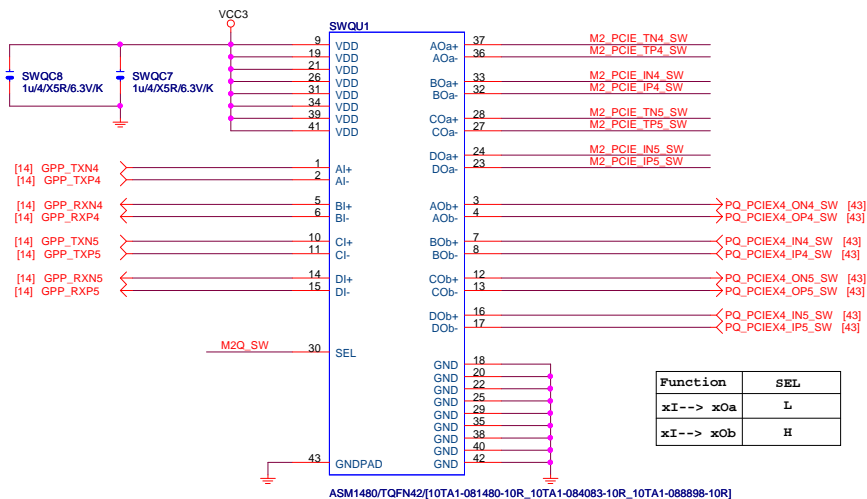
M2 HEATSINK

SMD螺柱 Footprint : HOLE_C236D165-A

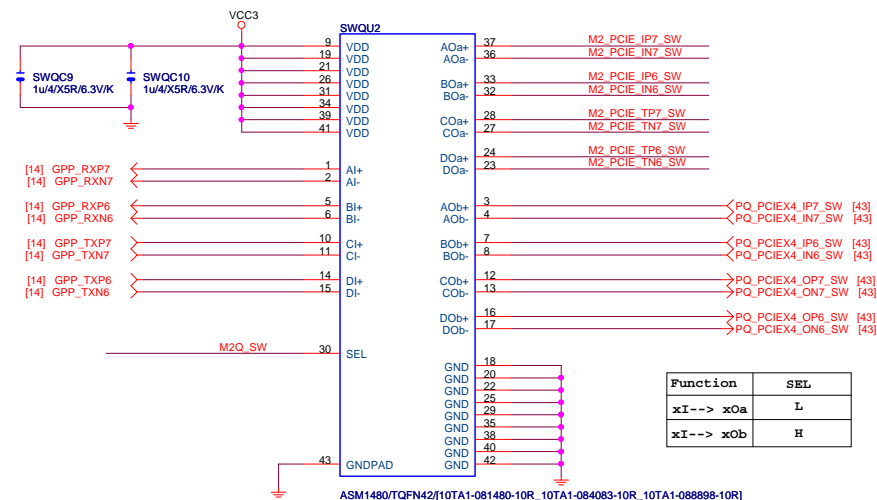
DIP螺絲
W/O M2_HS

CR[12KS2-110202-01R]

Rev 0.2



Function	SEL
xI--> xOa	L
xI--> xOb	H



Function	SEL
xI--> xOa	L
xI--> xOb	H

M2Q_SW	Output
H	PCIEX4
L	M.2
同時插	M.3

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PCIE SWITCH			
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